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PYROELECTRIC/INTEGRATED CIRCUIT INFRARED IMAGING ARRAY DEVELOPMENT

A. BOORNARD, et al.

RCA

TECHNICAL REPORT AFAL-TR-73-258

June 1973

Air Force Avionics Laboratory
Air Force Systems Command
Wright-Patterson Air Force Base, Ohio 45433

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PYROELECTRIC/INTEGRATED CIRCUIT INFRARED IMAGING ARRAY DEVELOPMENT

Final Technical Report

(22 Feb 1972 — 30 May 1973)

A. Boornard, D. Hall, E. Herrmann,
R. D. Larrabee, W. Morren, P. D. Southgate and
W. L. Stephens

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June 1973

FOREWORD

The work reported in this Final Technical Report was performed under Air Force Contract No. F33615-72-C-1804, entitled "Uncooled IR Image Mosaic Development", by the RCA Advanced Technology Laboratories of the Government and Commercial Systems Division, Camden, N.J., and by the RCA Laboratories, Princeton, N.J.

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The views and conclusions contained in this document are those of the authors and should not be interpreted as necessarily representing the official policies, either expressed or implied, of the Advanced Research Projects Agency or the U.S. Government.

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This report covers work performed from 22 February 1972 through 30 May 1973.

This technical report has been reviewed and is approved.

Amos Dicke
Electro-Optic Device Branch
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ABSTRACT

The development of techniques leading to the fabrication of thin polycrystalline triglycine sulfate films and their resulting characteristics as infrared detectors are described. The processing technology required to fabricate pyroelectric/integrated circuit thermal imaging arrays consisting of thin flim triglycine sulfate detectors on field effect integrated circuits is reviewed. The primary approaeh pursued under this program to the problem of providing the required high degree of thermal isolation between the detectors and the silicon substrate was to preferentially etch away the silicon underlying the detectors. In the resulting configuration, the thin thermally grown silicon dioxide membrane remaining after thc etching process serves to support the detector. A second thermal isolation technique, in which a thin, permanently poled, single crystal section of TGS is positioned above its companion two-dimensional integrated circuit substrate, is also described. In this arrangement the resulting air gap provides the thermal isolation; eontacts to the array detectors are made by means of vacuum deposited microfinger springs. The problem of providing thermal isolation proved to be the most diffieult obstacle eneountered during the program. No completely satisfactory approach evolved; as a result the objective of quantitatively assessing the performance of a small (16-by-16) element image sensor array was not met. The relative merits and shortcomings of X-Y and bucket brigade addressed pyroelectric sensor arrays are reviewed. The bucket brigade approach is shown to be a workable concept, with one 16-by-16 bucket brigade array having been fabricated and qualitatively assessed. An analysis of the performance eapabilities of X-Y and bueket brigade addressed thin film pyroelectric arrays was performed. The results indicate that a system noise equivalent temperature difference of 0.42° C at 10 frames/second with F/1 opties should be achievable in an X-Y addressed array consisting of 10-μm thick detectors 4 mils on a side and spaced on 8-mil centers. A noise model for a comparable bucket brigade array was developed, and results indieate a degradation in noise equivalent temperature difference by a faetor of 4.7 relative to the X-Y addressed array. However, the noise model may be greatly overestimating the noise; noise equilvalent temperature differences elose to those predicted for X-Y addressed arrays should be possible.

GLOSSARY OF ABBREVIATIONS

BB	bucket brigade
D	drain region of an FET
FET	field-effect transistor
FPN	fixed pattern noise
G	gate region of an FET
IC	integrated circuit
LSI	large scale integration
MOS	metal-oxide-semiconductor
NEΔT	noise equivalent temperature difference
PMOS	p-channel MOS
S	source region of an FET
SiO_2	silicon dioxide
S/N	signal-to-noise voltage ratio
TGS	triglycine sulfate

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Imaging Array Development

Air Force Contract No. F33615-72-C-1804
Sponsored by
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ARPA Order No. 1916
Final Technical Report
Period 22 February 1972 — 30 May 1973

The objective of this program was to develop the technology required for the fabrication of large scale uncooled two-dimensional pyroelectric/integrated circuit arrays suitable for passive infrared imaging over the 8- to 14-μm transmission window of the Earth's atmosphere. The pyroelectric detector material of principal interest was the organic compound triglycine sulfate (TGS), selected because of its high figure of merit for passive infrared imaging applications.

The pyroelectric detector arrangement selected for implementation in two-dimensional arrays consists of a thin section (10- to 25-μm thick) of either polycrystalline or single crystal TGS sandwiched between two thin film electrodes. The resulting detector configuration, essentially a minute temperature-sensitive capacitor, forms a sensitive detector of infrared radiation. An infrared image, when focused on an array of such detectors, will produce a spatial temperature distribution corresponding to the intensity of the radiation emitted by the scene. The spatial temperature distribution is accompanied by a change in the spontaneous electrical polarization of each detector element, which produces a pyroelectric signal voltage proportional to the scene radiation.

The pyroelectric effect has emerged as an attractive mechanism upon which to base passive infrared imaging systems. The most noteworthy features of pyroelectric detectors are operation at room temperature, which obviates the need for a cryogenic environment, and the potential to form two-dimensional arrays, which would circumvent the need for complex optomechanical scanners. The lack of a refrigerator and optomechanical scanner should assure large savings in system size, weight, cost, and complexity, and should result in highly improved reliability. Although lacking in sensitivity as compared with infrared imaging systems which utilize cryogenically cooled linear arrays of quantum detectors (such as mercury cadmium telluride or gold doped germanium), the advantages noted would allow the use of pyroelectric infrared imaging systems in applications where cryogenically cooled scan systems are not feasible.

The primary approach selected for the development of pyroelectric/integrated circuit arrays was to form a mosaic of individual delineated polycrystalline TGS detectors over a silicon integrated circuit substrate which contains the necessary detector sampling field effect transistors (FETs) and the required address and signal output lines. Key development problems included the formulation of suitable photolithographic and etching techniques to delineate thin TGS films into individual detectors, and the formulation of techniques to provide a high degree of thermal isolation of the detectors from the integrated circuit substrate. Progress in these areas is described in Section II of the report, in which the basic polycrystalline TGS materials work is also described.

Thermal isolation is particularly important since, without adequate isolation, degradation in detector voltage responsivity and accordingly poor temperature resolution capability will result. The thermal isolation technique applicable to polycrystalline TGS films requires preferentially removing (by chemically etching away) the portions of the silicon substrate under each row of detectors up to the thermally grown silicon dioxide (SiO_2) layer which covers the integrated circuit. In this manner, the detectors are supported on top of the thin SiO_2 membrane (12,000-Å thick). Detector heat loss by conduction to the remaining substrate material is greatly diminished, owing to the high thermal resistance of the thin SiO_2 membrane. This thermal isolation arrangement is illustrated in Section II and analyzed in considerable detail in Section V, in which the thermal time constants are calculated and in which the thermal conductance is calculated as a function of detector size, detector center-to-center spacing, and SiO_2 membrane thickness.

A second approach toward realizing pyroelectric/integrated circuit arrays, which utilizes a thin slab of single crystal TGS (about 25-μm thick), was also experimentally investigated. This approach uses the same integrated circuit substrates, but the undelineated detector array -- formed on a single crystal slab -- is positioned above the integrated circuit by means of thin shims located at the periphery of the array. Electrical contact to the array detectors is established by thin film microfingers made of bimetallic vacuum-deposited strips; these form minute curled springs, attached to the substrate, which contact the array. The air gap between the TGS detector section and the silicon substrate thermally isolates the detectors from the substrate. This arrangement is described and analyzed in Section III.

Two types of infrared imaging circuit arrays were investigated, an X-Y addressed array and a bucket brigade array: both were designed to contain 16-by-16 pyroelectric detector elements, each measuring about 4 mils on a side, with a center-to-center spacing of 8 mils in both the x- and y-directions. The pyroelectric material may be either polycrystalline or single crystal in either type of array.

The X-Y addressed array contains a TGS detector element and two FETs within each sensor cell: a signal FET and a reference FET. This arrangement permits extraction of low level pyroelectric signals by subsequent amplification in difference

amplifiers located external to the imaging array. The array would be shuttered (at rates of 10/second to 30/second) and digitally addressed one column at a time.

The bucket brigade array is the pyroelectric counterpart of the visible light bucket brigade image sensor array. Each sensor cell contains a pyroelectric detector capacitor, a metal oxide semiconductor (MOS) capacitor, and two FETs. The pyroelectric induced charge, which is proportional to the scene radiation, is transferred from cell to cell along a series of linear bucket brigade arrays which comprise the two-dimensional array. The bucket brigade array is described in Section IV and an analysis of the performance of X-Y addressed and bucket brigade pyroelectric sensor arrays is presented in Section V.

Section I
INTRODUCTION

The pyroelectric effect (i.e., the temperature induced change in spontaneous polarization of certain materials) is an attractive mechanism upon which to base passive thermal imaging systems. Its most desirable features are operation at room temperature, which obviates the need for providing a cryogenic environment, and the potential for forming two-dimensional arrays, which would circumvent the need for complex optomechanical scanners. The lack of a refrigerator and optomechanical scanner would assure large savings in size, weight, cost, and complexity and should result in highly improved reliability. Although lacking in sensitivity as compared with thermal imaging systems which utilize cryogenically cooled linear arrays of quantum detectors (such as mercury cadmium telluride and tin telluride or gold doped germanium), the advantages noted would permit the use of pyroelectric thermal imaging systems in applications where cryogenically cooled scan systems are not feasible.

This program was carried out to develop the technology required for the fabrication of large scale, two-dimensional pyroelectric/integrated circuit detector arrays suitable for imaging over the 8- to 14-μm transmission window of the Earth's atmosphere. The approach of primary interest was to form a mosaic of delineated pyroelectric detectors (of polycrystalline material) over a silicon integrated circuit substrate containing the necessary addressing and/or readout circuitry. An object of the program was to fabricate and evaluate a small two-dimensional array of pyroelectric sensor elements.

Two types of arrays were investigated, an X-Y addressed array and a bucket-brigade (BB) array; both of these were designed to contain 16-by-16 pyroelectric detector elements, each element measuring about 4 mils on a side, with a center-to-center spacing of 8 mils in both the x- and y- directions.

A second approach was to utilize the same integrated circuit substrates but to form the detectors on a thinned single crystal slab of the pyroelectric material mentioned above the integrated circuit substrate and contacted to the substrate by means of thin film metallic microfingers.

Since pyroelectric detectors are heat-sensitive elements, effective thermal isolation of the detectors from the integrated circuit substrate must be provided if high

array sensitivity is to be obtained. Additionally, delineation of the detector elements is also desirable in order to obtain the least thermal crosstalk, or equivalently to realize the highest spatial resolution possible.

The problem of providing thermal isolation of the detector elements from the silicon integrated circuit substrate was the major technical difficulty encountered during the program. A novel thermal isolation technique was devised, but the necessary technology was not fully developed. As a result, our objective of quantitatively assessing a small two-dimensional image sensor array was not met. Arrays without thermal isolation were built early in the program using undelineated polycrystalline triglycine sulfate (TGS) on a PMOS integrated circuit substrate. An observable pyroelectric response was obtained but performance was poor owing to severe degradation in voltage responsivity caused by loss of heat into the silicon substrate.

A. PYROELECTRIC EFFECT

Certain materials exhibit a spontaneous electrical polarization, an alignment of the internal electric dipoles, even in the absence of an applied electric field. The polarization decreases with increasing temperature and vanishes at a specific temperature, called the Curie temperature after the analogous behavior in ferromagnetic materials. Because the polarization is temperature dependent, materials exhibiting this property are called pyroelectric. The polarization temperature dependence of triglycine sulfate (TGS), a material of particular interest to this program, is illustrated in Fig. 1-1. Measurements of the rate of change of polarization with respect to temperature, dP/dT, known as the pyroelectric coefficient, range from 3.5×10^{-8} coulombs/cm^2 - ^oK at 27^oC to 1×10^{-7} coulombs/cm^2 - ^oK at 40^oC for single crystal TGS.[1,2] Other properties of single crystal TGS are listed in Table 1-1. Polycrystalline TGS, which forms the basis for the primary pyroelectric/integrated circuit approach described in this report, has properties which differ from those of the single crystal material. The differences and their effects are discussed in various sections of the report (e.g. Section II. A, Table 2-2, and Section V).

An external electric field is not normally observable in the vicinity of a pyroelectric material, even if it is an insulator, because the polarization field ultimately becomes neutralized by leakage currents and/or by stray charges which are attracted to and bound to the surface. The bound surface charge is unable to respond to rapid changes in the polarization. Thus, a sudden temperature-induced change in the polarization will be accompanied by an observable external electric field while the surface charge is adjusting to the new conditions. It is this transient electric field that forms the basis of the pyroelectric detectors to be discussed.

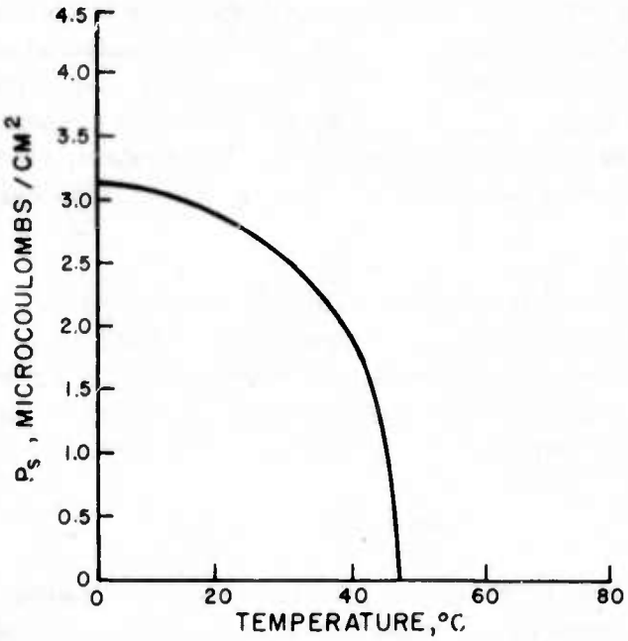


Fig. 1-1. Spontaneous polarization of TGS as a function of temperature (from Refcrence 2).

TABLE 1-1. SELECTED PROPERTIES OF SINGLE CRYSTAL TRIGLYCINE SULFATE AT 300° K (After Putley, Ref. 1)

Pyroelectric Coefficient, dP/dT	$2\text{-}3.5 \times 10^{-8}$ C/cm^2 - °K
Relative Dielectric Constant, ϵ_r	25 - 50
Diclectric Coefficient, ϵ	$2.1 - 4.42 \times 10^{-12}$ F cm^{-1}
Specific Heat, C_p	0.97 J/gm-° K
Thermal Conductivity, K	6.8×10^{-3} W/cm-° K
Mass Density, ρ_m	1.69 gm/cm^3
Thermal Diffusivity	0.41×10^{-2} cm^2/s

B. PYROELECTRIC DETECTORS FOR THERMAL IMAGING

The pyroelectric effect can be utilized to form a sensitive infrared detector by eonstructing a parallel plate capacitor with the pyroelectric matc.ial as the diclectric. The absorption of infrared radiation results in a temperature-induced change in the

polarization which is accompanied by a transient change in the potential across the detector electrodes. A pyroelectric detector, with its associated high input resistance and low input capacitance FET amplifier, is shown in Fig. 1-2. The resistance, R_d, which shunts the capacitance, C_d, of the detector is always present by virtue of the leakage resistance of the pyroelectric material. The transient electric field that develops when the detector is subjected to radiation can be detected by the voltage drop across R_d.

For application to infrared imaging systems, the detector RC time constant should be large compared with the frame time to ensure negligible loss of charge during exposure. In this mode of operation, the detector integrates the infrared scene radiation for the total exposure, and to a first approximation the change in the detector open-circuit voltage, ΔV, is proportional to the change in temperature, ΔT.

$$\Delta V \approx \Delta Q / C_d \tag{1-1}$$

where ΔQ is the temperature-induced change in charge on the detector electrodes in coulombs and C_d is the capacitance of the detector in farads. C_d is given by

$$C_d = \frac{\epsilon A_d}{d}$$

Here A_d is the area of the capacitor plates in square centimeters, d is the thickness of the pyroelectric material in centimeters and ϵ is the dielectric coefficient of the pyroelectric material in farads/centimeter.

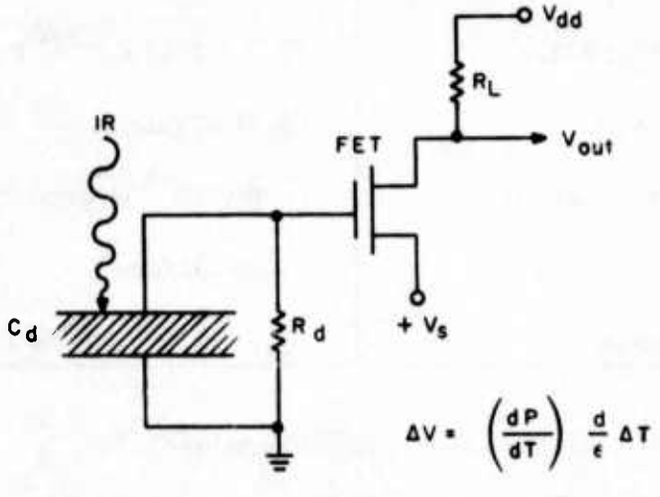


Fig. 1-2. Basic arrangement of a pyroclectric thermal detector.

Since the polarization is equivalent to the charge per unit area,

$$\Delta Q \approx \frac{dP}{dT} A_d \Delta T \tag{1-2}$$

which leads to

$$\Delta V \approx \frac{dP}{dT} \frac{d}{\epsilon} \Delta T \tag{1-3}$$

The expression for ΔV shows that for thermal imaging arrays, an applicable figure of merit for the pyroelectric material is $(dP/dT)\frac{1}{\epsilon}$. Triglycine sulfate was selected because it has one of the highest known figures of merit. [1,3]

Because the dielectric constant of TGS increases with increasing temperature along with the pyroelectric coefficient, the dependence of this figure of merit on temperature is less than the dependence of the pyroelectric coefficient, and to a first approximation is almost independent of temperature from somewhat below room temperature to just below the Curie temperature. Consequently, the necessity of accurately controlling the operating temperature is not as serious as would first be thought from an examination of Fig. 1-1.

Note that a pyroelectric detector has no response to a steady signal (i.e., ΔQ of Eq. (1-2) leaks away through R_d of Fig. 1-2 with a time constant equal to $R_d C_d$). This means that it is necessary to view the scene alternately with a reference (uniform temperature) scene so that the detector output will be proportional to the difference between the scene and reference temperatures. One inherent advantage of this mode of operation is that the detector is insensitive to the background radiation (herein defined as that portion of the radiation from the background equivalent to the reference temperature) because it is, in effect, a steady signal. This relaxes the severe uniformity of response requirements that sensitivity to background imposes on quantum detectors, and would make pyroelectric thermal imaging arrays capable of operating without the necessity of elaborate gain control (responsivity equalizing) schemes.

C. POLYCRYSTALLINE APPROACH

In order that the incident scene radiation increase the temperature of the detector elements as much as possible, it is necessary that the detector thickness be no greater than that required to absorb the radiation, and that the detector elements be thermally isolated from their surroundings. Using appropriate values for TGS,[1,4] it is found that a good compromise design occurs when the detector material is about 10-μm thick. This thickness is attainable with polycrystalline TGS films but it is smaller than is permitted by the present state of the art for unsupported single crystal TGS. The polycrystalline approach also inherently provides a way to obtain thin uniform pyroelectric layers that can be readily deposited on large area thin film integrated circuit substrates.

The technique for providing thermal isolation of polycrystalline TGS detectors from the silicon integrated circuit substrate upon which the detectors are formed is illustrated in Fig. 1-3, which shows a delineated polycrystalline TGS detector supported by a thin thermally grown silicon dioxide membrane that remains after the silicon under the detector has been preferentially etched away. In this manner loss of heat from the detector to the silicon is greatly reduced since the heat must be conducted sideways along the thin silicon dioxide membrane.

The polycrystalline approach is not as degrading as might be expected because once poled, all the components of spontaneous polarization of the individual grains in the poling direction add coherently and only their perpendicular components are ineffective. The resulting degradation in detector voltage responsivity is calculated to be less than a factor of two as compared to single crystal detectors. Some advantages of polycrystalline detectors that tend to compensate for this relatively small loss in responsivity are:

1) Small inhomogeneities in the parent pyroelectric source material are averaged out in a composite layer, thus providing a technique for producing large areas of uniform photoresponse without having to impose severe restrictions on the permissible inhomogeneity of the source material.

2) Since the procedures for preparing a single detector are virtually identical to those for arrays of many detectors, this approach is ideally suited for multielement imaging arrays.

3) Some important film properties (e.g. resistivity) can, in principle, be independently controlled by judicious choice of fillers and/or "glue" used to cement the component pyroelectric particles into a coherent film.

Some problems associated with polycrystalline detectors should be noted. Although uniform in their electrical properties and capable of being formed on virtually any substrate, pyroelectric films are difficult to prepare and a number of time-consuming steps are required. Additionally, while single crystal TGS can be permanently poled, as for example by the addition of l-alanine,[5] no technique is presently known for permanently poling polycrystalline pyroelectric films. However, it has been found that when polycrystalline TGS films are doped with glycolic acid broadening of their hysteresis loops occurs. This might result in an improvement in their electrical properties such as the loss tangent and possibly the pyroelectric coefficient.

D. SINGLE CRYSTAL APPROACH

The use of single crystal material in a pyroelectric/integrated circuit array requires contacting each of the detector elements formed on the thin "freely-supported"

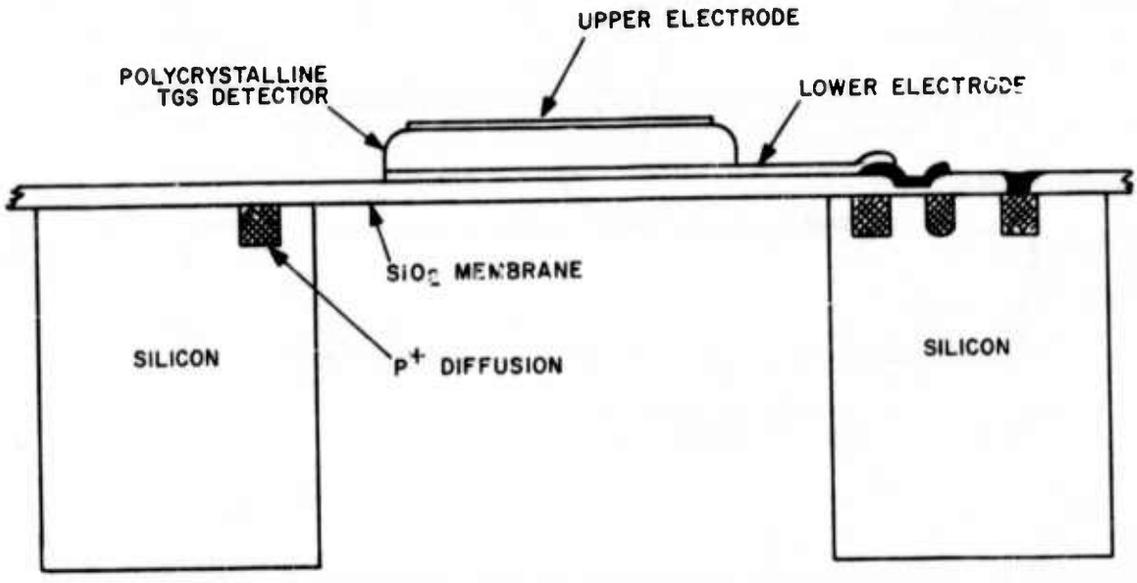


Fig. 1-3. Arrangement of a single sensor cell of a polycrystalline TGS detector array illustrating the thermal isolation technique.

section of single crystal material to the silicon integrated circuit substrate. Conceptually, this can be accomplished using thin metallic film microfingers. Since thermal isolation is provided by the air gap separating the single crystal pyroelectric slab from the integrated circuit, etching of the silicon substrate is not required. The approach is suitable for use in either X-Y addressed or bucket brigade arrays. The basic arrangement for achieving thermal isolation of the sensor portion of the array from the integrated circuit is illustrated in Fig. 1-4, which shows a cross-sectional view of a thin single crystal sheet of TGS contacted by means of microfingers to the integrated circuit substrate. A high degree of thermal isolation is provided by the air gap with the thin long microfingers contributing little in the way of heat sinking.

An advantage of the single crystal approach is that it permits the use of permanently poled pyroelectric materials. Problems associated with the single crystal approach include the development of techniques to reproducibly obtain the thin metallic microfingers, and the development of techniques to further reduce the thickness of single crystal TGS (presently about 25-μm thick) in order to improve the voltage responsivity. Additionally, ways must be found to produce uniform permanently poled materials. The problem, to date, has been that small regions of opposite polarization are formed.

E. PYROELECTRIC THERMAL IMAGING SYSTEM

The manner in which a pyroelectric array would be utilized in a thermal imaging system is illustrated in block diagram form in Fig. 1-5. The infrared scene radiation, after passing through the aperture of a continuous motion shutter, is focused onto the

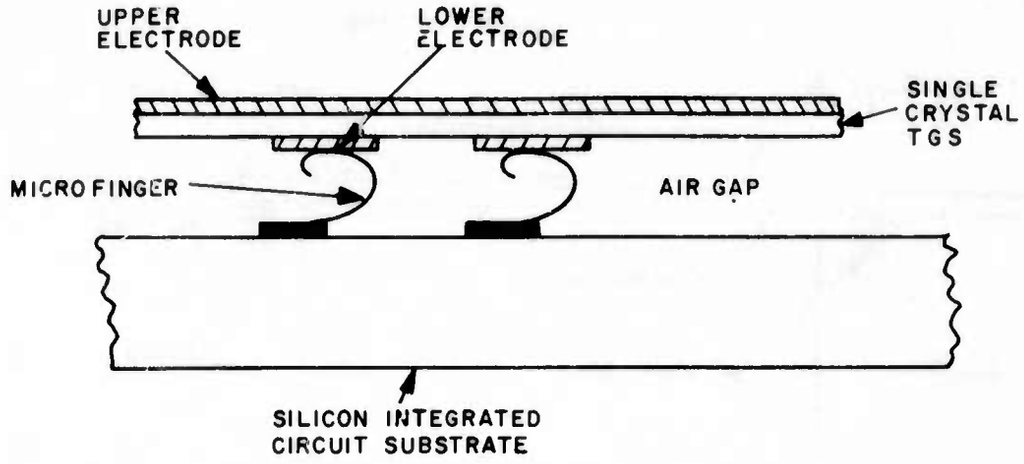


Fig. 1-4. Thermal isolation technique for the single crystal TGS array.

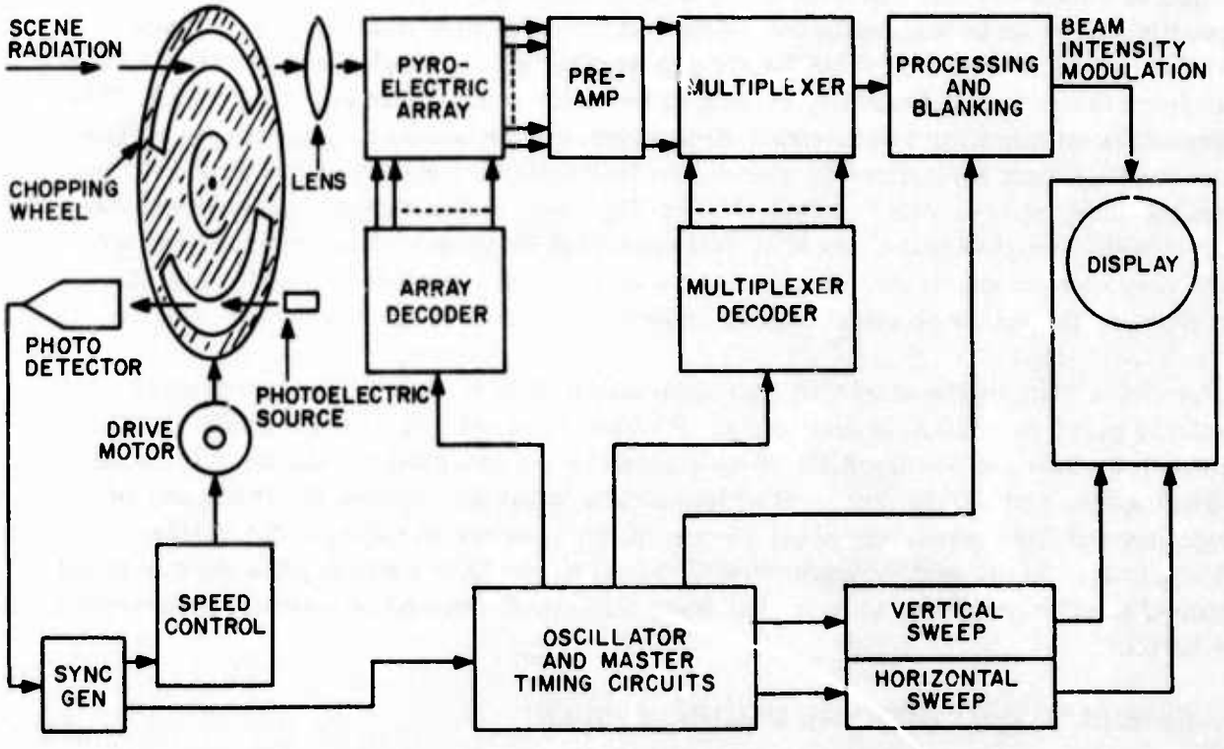


Fig. 1-5. Block diagram of a pyroelectric thermal imaging system.

two-dimensional pyroelectric array. As the opaque portion of the shutter covers the first exposed column of detectors readout of the array is begun, one column at a time. Each column of detectors receives the scene radiation for the full exposure period. In an X-Y addressed array, the pyroelectric signals derived from each column of detectors are simultaneously amplified and then multiplexed to form a corresponding line of scene information on the display. The sequence is repeated with each column of detectors being addressed. In a bucket brigade array, each column of detectors forms part of a bucket brigade register that can be individually read out by activating its clock lines. Calculations indicate that an array of polycrystalline TGS detectors, each 4 mils on a side and on 8-mil centers should be capable of achieving noise equivalent temperature differences of 0.42°C, 0.48°C, and 0.53°C at frame rates of 10/s, 20/s and 30/s, respectively.

The remaining sections of this report will describe the progress made in developing the technology required to realize the pyroelectric/integrated circuit array approaches mentioned herein. Section II will discuss the progress made in forming polycrystalline TGS films, delineating the films into individual detector elements, obtaining continuous metallization of the upper electrodes, and in providing thermal isolation by preferential etching of the silicon substrate. Section II also summarizes the properties of polycrystalline TGS films. Section III describes the single crystal pyroelectric array. Section IV discusses operation of bucket brigade and X-Y addressed pyroelectric imaging arrays. In Section V an analytical assessment is made of the performance capabilities of arrays containing polycrystalline TGS detector elements.

Section II

POLYCRYSTALLINE TRIGLYCINE SULFATE DETECTOR ARRAY FABRICATION TECHNOLOGY

A large body of new technology had to be developed before one could consider fabricating the pyroelectric/integrated circuit thermal imaging arrays outlined in Section I. A basic premise employed in developing these new technologies was to avoid disturbing the well-established PMOS (p-channel metal-oxide-semiconductor) processes by restricting all new procedures to before and/or after conventional processing. Table 2-1 summarizes the main sequence of steps that have evolved for processing blank silicon wafers into finished and packaged arrays. The procedures outlined in step 1 of Table 2-1 are required to facilitate step 3, which follows after completion of the conventional PMOS processing. These initial procedures do not interfere with PMOS processing since they are mainly concerned with crystallographic alignment and the condition of the back (or inactive) side of the silicon wafer. Figure 2-1 is a photograph of a wafer of 16- by 16-element bucket brigade mosaics of the type discussed in Section IV as it appears after PMOS processing (i.e. after step 2 in Table 2-1).

This section of the report is concerned with the problems of hybridizing polycrystalline pyroelectrics with integrated circuits and with the specific details of their solution as represented by steps 3, 4, and 5 of Table 2-1. The new technologies developed for fabricating the thermal isolation structure shown in Fig. 1-3 and for depositing, delineating, and metallizing triglycine sulfate films will be covered in detail in Sections II.B and II.C. This discussion will include an outline of the work remaining to be done in these two main technological development areas and will cover some compatibility problems that might arise when delineation is attempted in pyroelectric layers deposited on top of substrates containing the thermal isolation structure.

A. HYBRIDIZING PYROELECTRIC DETECTORS WITH INTEGRATED CIRCUITS

1. Polycrystalline Pyroelectrics as Mosaic Detectors

Polycrystalline triglycine sulfate (TGS) films consist of randomly oriented grains that collectively show little or no preferred orientation. It is therefore necessary to pole the material to align all of the spontaneous polarization vectors of the

TABLE 2-1. OUTLINE OF ARRAY FABRICATION PROCESSING STEPS

1.	Select silicon wafers with the desired crystallographic orientation, optically polish and grow a thermal oxide on the back side, and provide an alignment slot on the front side.
2.	Construct the desired integrated circuit by conventional PMOS processing techniques.
3.	Provide the necessary structure for thermally isolating the individual detectors from the silicon substrate.
4.	Deposit a uniform pyroelectric layer over the structure and delineate it into a mosaic of individual detectors.
5.	Evaporate metal contacts over the top of each detector.
6.	Dice the wafer into individual chips of arrays and package them into suitable holders.

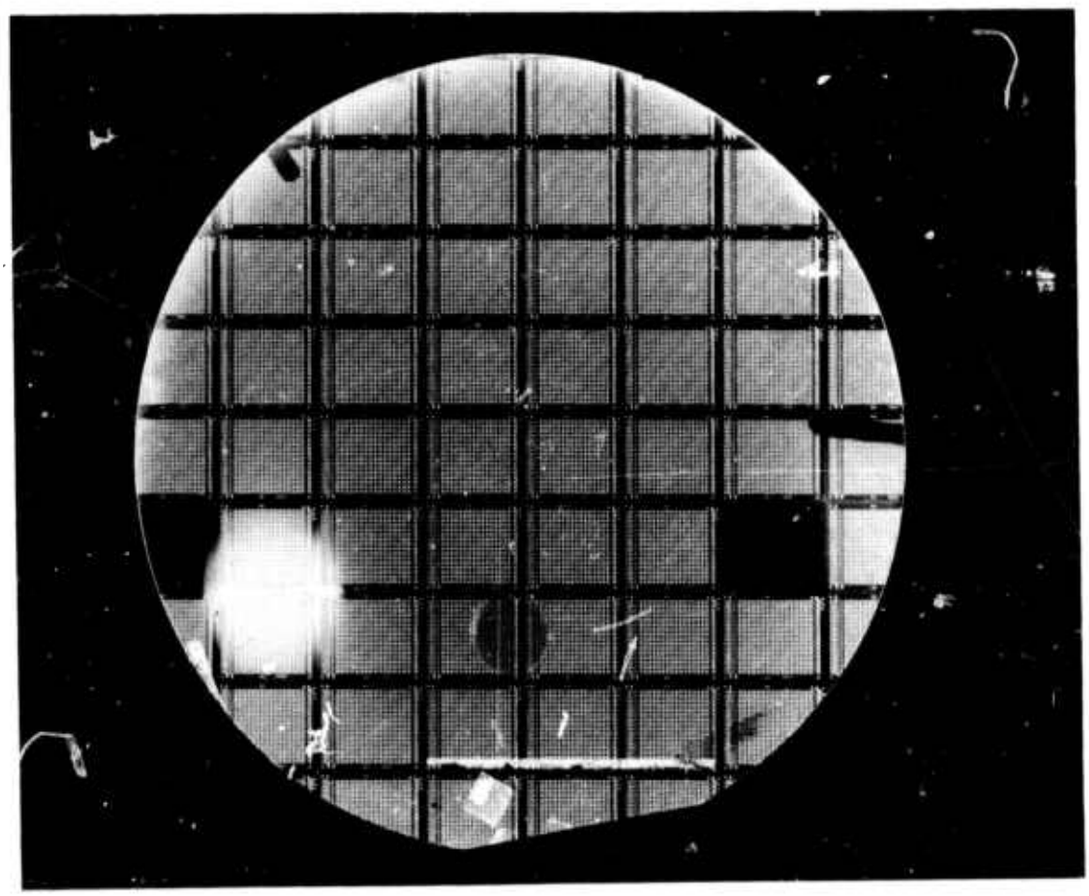


Fig. 2-1. Photograph of a silicon wafer containing a series of bucket brigade readout circuits for 16- by 16-element pyroelectric imaging mosaics.

individual grains so that their components perpendicular to the parallel plate electrodes of the detector capacitor are oriented in the same direction. If this is not done, the polycrystalline films produce no output voltage when heated. Poling is accomplished by applying a dc voltage to the TGS detector-capacitor, either at room temperature or while cooling it through its Curie temperature (49°C for TGS).[1,6]

Figure 2-2 shows how the voltage responsivitiy (a measure of the degree of alignment of the spontaneous polarization vectors of the individual grains) of a large area polycrystalline TSG detector (fabricated by the techniques to be discussed in Section II.C to follow) was observed to vary with the average dc electric field during

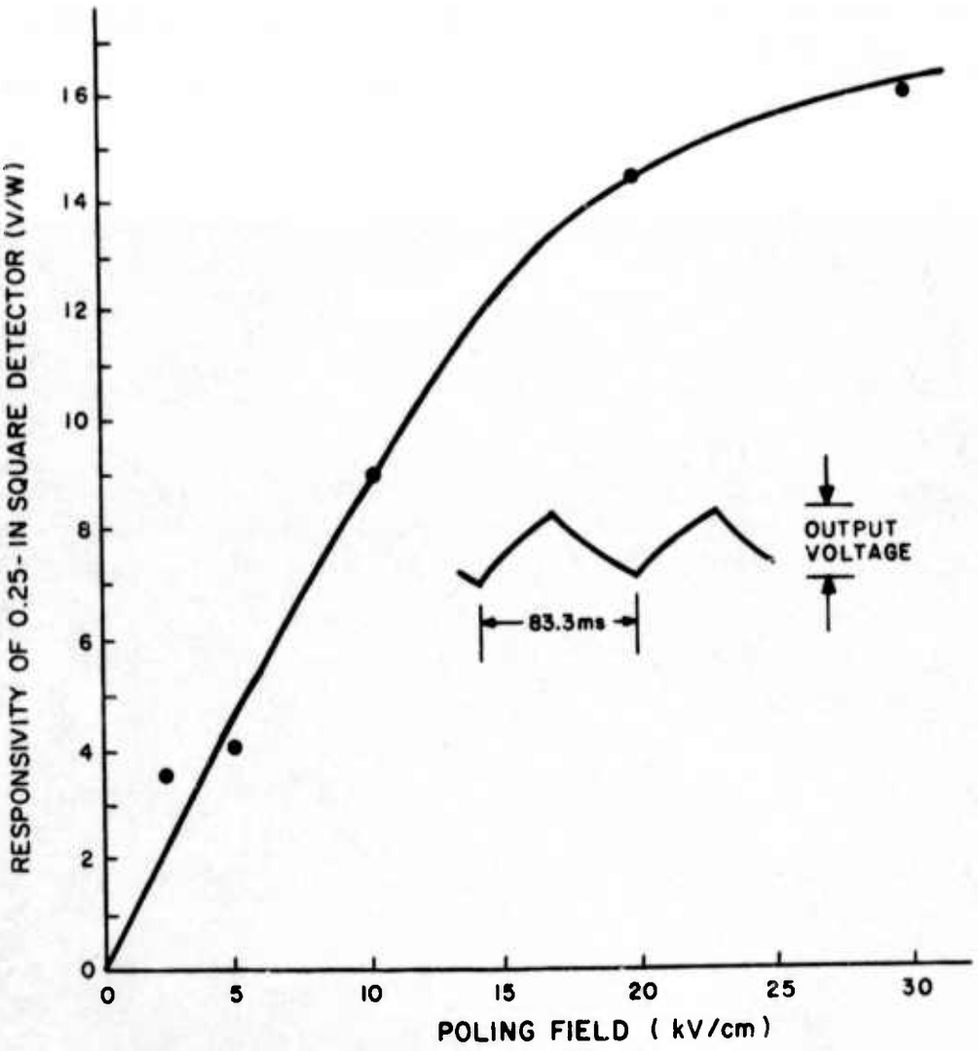


Fig. 2-2. Voltage responsivity of a large area polycrystalline triglycine sulfate (TGS) detector on a glass substrate as a function of poling electric field intensity.

room-temperature poling. Electric fields in excess of 30 kV/cm are required for saturation polarization. Unlike single crystals, polycrystalline films are slow to respond to the poling field, often requiring up to an hour to reach steady-state polarization at room temperature. The poling fields of Fig. 2-2 were applied until no further increases in responsivity could be detected. After observing the data of Fig. 2-2, the poling field was removed and the sample was placed in a nonhermetic box and set aside (i.e., in ordinary room air) for a life test. For several months the responsivity was carefully monitored and found to remain constant. In fact, over a year later, the responsivity was still about the same, thus clearly illustrating two important properties of the polycrystalline films:

1. They do not exhibit the tendency for spontaneous depolarization at room temperature that is often observed in single crystal material.

2. They are stable in air at ordinary room temperature (at normal humidity levels) for at least one year.

Consequently, it is concluded that polycrystalline films will present minimal storage problems and will not require frequent repoling during use. However, the film will become depoled if heated above its Curie temperature and subsequently cooled to room temperature without any poling field applied. In that event, the film can be repoled by simply reapplying the dc poling field.

The effects of polycrystallinity can be estimated by performing a spatial averaging of the pertinent properties over all possible grain orientations. In the case of the pyroelectric coefficient (i.e., dP/dT of Eq. (1-3)), one calculates that its average component along the poling axis is one-half the single crystal value. Computation of the effective dielectric constant, ϵ, is more complicated since TGS has uncqual components of its dielectric constant along its three principal axes.[6] However, if the components are all independently averaged and added together, one obtains a value that is about 0.67 of the value along the polar axis. Consequently, the figure of merit (i.e., $1/\epsilon$ dP/dT) for TGS is reduced by only a factor of 1.33 (i.e., 0.67/0.50) by the randomness introduced by polycrystallinity. The present densification technique produces films with an estimated 80% of bulk density. Since film porosity lowers both ϵ and the polarization proportionally, it has no direct effect on the detector responsivity. Porosity and polycrystallinity, however, do reduce the effective capacitance of a TGS detector and the net charge produced in response to a given temperature change, thus tending to enhance the degrading effects of any shunting capacitance. The amount of degradation is proportional to the ratio of shunt capacitance to detector capacitance and therefore is only of prime importance for small detectors (for example those in the arrays of Fig. 2-1, but not in the case of the large area test detectors used to obtain the data for Fig. 2-2).

Absorption of infrared radiation in the semitransparent top electrode (Fig. 1-3) is not degrading if the frame time is sufficiently long to permit the heat to

be conducted into the TGS dielectric. Since the thermal conductance of the present porous TGS layers has not been measured, it is not possible to give quantitative estimates of the time required for this heat flow. However, for films of the anticipated 10 to 20 micrometers thickness, it is estimated that redistribution of heat will be effective for any reasonable frame rate of current interest (i.e. for frame rates less than 50 per second). Reflection from the top electrode does represent a real loss and thus a degradation in performance. Experimentally, it is found that an aluminum top electrode with a sheet resistance of about 1 ohm/square degrades the performance of test detectors by a factor of two (the surface granularity of the polycrystalline films helps to inhibit reflection). Since the detectors are connected to high-impedance circuits (to provide the desired open-circuit mode of operation), sheet resistances much larger than 1 ohm/square are acceptable and seem to introduce little degradation.

Some measured and/or calculated properties of polycrystalline TGS films deposited by the techniques to be discussed below are summarized in Table 2-2 and compared with published values for single crystal material. It can be seen from this table that the effects of polycrystallinity are not very degrading and, in the case of thermal conductivity, may actually be helpful in permitting reasonable levels of thermal isolation without actually delineating the TGS film into individual detectors (i.e., the mosaic of detectors could be defined by only a pattern of its metallic electrodes). The undesirable effects of shunting capacitance have been mentioned above and because of the reduced dP/dT, ϵ, and density, are somewhat more degrading in the polycrystalline case. Notice that without the thermal isolation structure of Fig. 1-3 (bottom), there would be significant shunt capacitance between the lower electrode and the underlying silicon substrate. For a 10-μm thick TGS detector mounted on a 12,000-Å silicon dioxide film, this would contribute a shunt capacitance that would be about equal to the actual detector capacitance and would thus reduce its output voltage (and thus its responsivity) by a factor of about two. Consequently, when the silicon is removed from under the detector for thermal isolation, (see Fig. 1-3), it also drastically reduces the shunting capacitance.

The test detector of Fig. 2-2 was designed to have a large area (0.25- by 0.25-in) and was mounted on an insulating substrate (5-mil thick glass) to minimize any degrading shunt capacitance effects (including the wiring and input capacitance of the field-effect transistor preamplifier to which it was connected). In addition, the TGS dielectric was made comparatively thick (20 μm) and the chopping rate was relatively fast (120 Hz) to reduce the relative importance of thermal loading of the glass substrate. Using published values for the thermal constants of single crystal TGS and glass (actually silicon dioxide[7]), one estimates that if there were no thermal resistance at the TGS-substrate interface, heat would penetrate about 28.6 μm into the glass substrate during the 1/240 second period that the shutter was either open or closed. Consequently, one estimates that about 2/3 of any heat that is initially absorbed by the TGS dielectric will be lost by conduction to the substrate. Using this factor of degradation, the temperature of the TGS detector will fluctuate by 2.8×10^{-5}°C when viewing a 500°K blackbody (which produces a total flux of 10^{-4} watts/cm^2 at the detector location) through

TABLE 2-2. COMPARISON OF POLYCRYSTALLINE AND SINGLE CRYSTAL TRIGLYCINE SULFATE

Parameter	Single Crystal Value[1,6]	Polycrystalline Value
Pyroelectric Coefficient $\left(\frac{dP}{dT}\right)$	2-3.5 x 10^{-8} coulombs/cm^2-°K	Calculated to be 1/2 the single crystal value*
Relative Dielectric Constant (ϵ)	43 along the polar axis and 8.6 and 5.7 along other axes (at 23°C)	Calculated value = 28.7* Measured value = 14.4**
Dielectric Loss Tangent	—	Measured Value = 0.1 (at 1 kHz)
Mass Density	1.69 grams/cm^3	Lower by densification factor of approximately 0.8
Specific Heat	0.97 joules/gram-°C	Lower by densification factor
Thermal Conductivity	6.8 x 10^{-3} joules/cm-s-°C	May be considerably lower because of film porosity
Electrical Resistivity	10^{12} ohm-cm	Measurements indicate: 10^{14} ohm-cm in dry air 10^{12} ohm-cm in room air

*Assuming bulk density
**At room temperature

the 120-Hz room-temperature, square-wave chopping wheel. Using Eq. (1-3) with dP/dT equal to 1.4×10^{-8} coulombs/cm^2°K and a relative dielectric constant of 28.7 (values appropriate for polycrystalline material-see Table 2-2), one estimates that this detector will produce a peak-to-peak terminal voltage of 0.314 mV. The expected voltage responsivity, therefore, is simply this voltage divided by the total power incident upon the detector (i.e., 0.41×10^{-4} watts) or 7.65 volts/watt. It is interesting to note that the output voltage from pyroelectric detectors is independent of area (as long as the effects of shunt capacitance can be neglected). If this detector were the same size as the detectors in the 16- by 16-element bucket brigade array (i.e., 5.5 mils by 3.5 mils), this same 0.314 mV would correspond to a responsivity of 24,800 volts/watt. However, because of the degrading effects of shunt capacitance, heat loss out the electrical connections, and the spreading of heat as it enters the substrate, an actual detector of this size would not be this good. Although over simplified, this example does show that small area pyroelectric detectors can attain quite high responsivities. The actual system responsivities expected for TGS mosaic detectors of various sizes and degrees of thermal isolation are discussed in Section V of this report.

At the highest poling field of Fig. 2-2, the measured responsivity of the large area test detector was 16 volts/watt or about 2.1 times the value computed above. This increase is attributed to reduced effectiveness of thermal loading of the glass substrate due to overestimating the thermal conductivity of the porous polycrystalline TGS films. If the thermal conductivity of polycrystalline TGS is assumed to be only 0.46 of the bulk value in Table 2-2, then the computed responsivity would agree with the measured value of 16 volts/watt. Although not intended to be a rigorous analysis, these results clearly indicate that the present polycrystalline layers are exhibiting about the responsivity one would expect based on the above arguments regarding polycrystallinity, thermal conductivity, and thermal isolation.

Consequently, it is concluded that the present technique of depositing polycrystalline TGS detectors directly upon an integrated circuit (containing the necessary addressing and/or readout circuitry) appears to be a viable approach to solid-state imaging in the infrared. In addition, the polycrystalline approach is inherently less sensitive to inhomogeneities in the starting material (they are all "averaged-out" in the final film), has less tendency to spontaneously depole, and is more suitable for large area applications than approaches based on single crystal detectors.

2. Techniques for Thermally Isolating the Detectors

In common with other types of thermal detectors, pyroelectric detectors must be provided with a high degree of thermal isolation from their surroundings. Without adequate thermal isolation, the detector's voltage responsivity becomes seriously degraded, resulting in poor sensitivity. Additionally, when arranged in array form, it becomes necessary to prevent thermal communication between detector elements in order to reduce thermal crosstalk to a minimum.

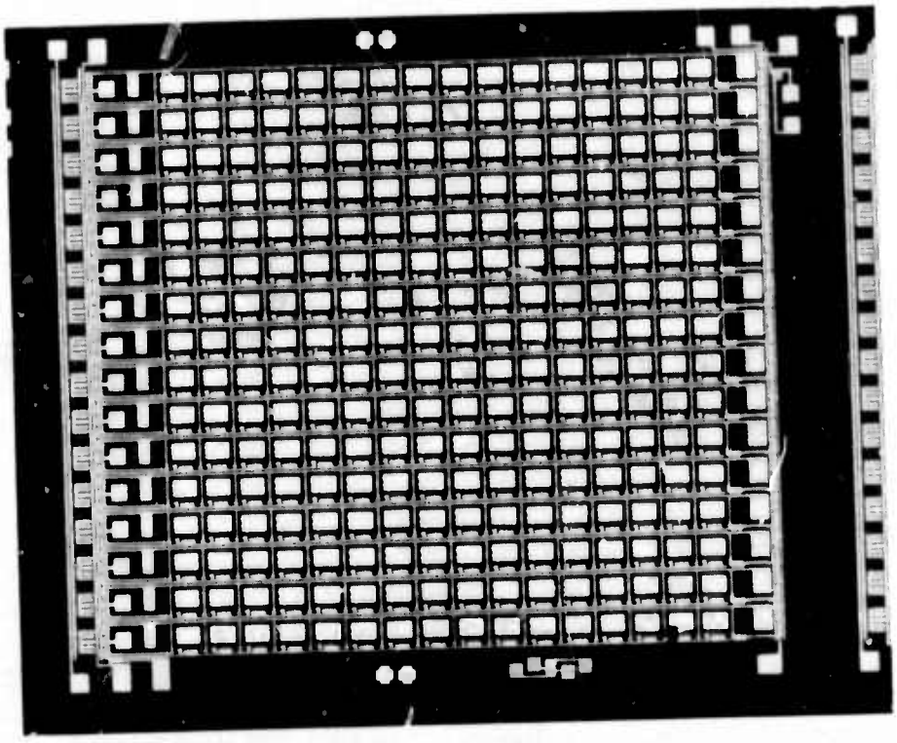


Fig. 2-3. Photograph of one 16- by 16-element bucket-brigade readout array from the wafer shown in Fig. 2-1.

A number of schemes for accomplishing thermal isolation between the detectors of the array and their surroundings have been proposed. However, only one has emerged as reasonable from the viewpoints of attainable performance and complexity of the new technologies required. This preferred approach is simply to remove the silicon from under the detectors and leave them supported by the thin silicon dioxide film previously provided for that purpose (See Fig. 1-3). The dominant heat loss mechanism in this arrangement is sideways conduction through the thin silicon dioxide film (and the electrode metallization) to the supporting silicon framework. By making the detectors smaller, one can increase the distance over which heat must flow and reduce this conductive heat flow to tolerable levels. These design considerations are presented in greater quantitative detail in Section V, where the expected performance of such thermally isolated arrays is assessed.

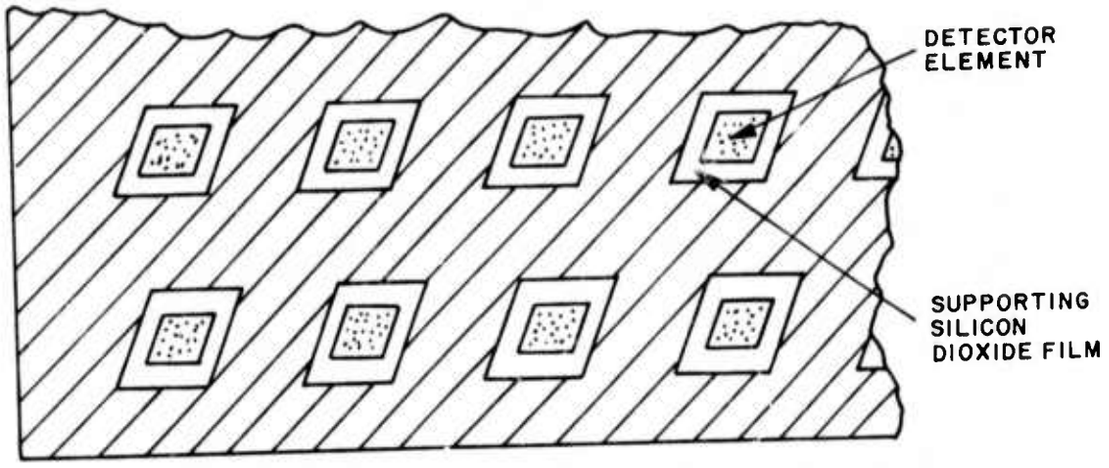
Figure 2-3 is a photograph of one 16- by 16-element bucket-brigade array from the wafer of Fig. 2-1. The locations of the individual detectors that will be subsequently deposited are framed-in by the horizontal and vertical clock lines and specifically marked by the large (5.5-mil by 3.5-mil) lower electrode pads. The associated bucket-brigade circuitry (i.e., one MOS capacitor and two field effect transistors) is completely contained in the horizontal space between the rows of detectors (see Section IV). Realization of the present thermal isolation scheme requires removal of the silicon from

under the lower electrode pads and sufficiently more to expose the required peripheral silicon dioxide supporting film (see Fig. 1-3), but not so much more as to remove portions of the circuitry in the remaining supporting silicon structure. It is apparent that silicon removal must be done with great precision (i.e., to within a tolerance of a fraction of a mil) and, since the silicon dioxide film covers the front (or active) side of the wafer, one is constrained to remove the silicon from the back (or inactive) side of the wafer. In addition, the delicate nature of the silicon dioxide film precludes mechanical removal techniques and leaves chemical etching as the only practical alternative. One can borrow the techniques of using infrared light to "see through" a silicon wafer, currently in use in the fabrication of beam leaded integrated circuits, to align a back-side mask to the front-side circuitry. However, one must achieve a high degree of control over the undercutting of the back-side etch mask in order to achieve the required fractional-mil dimensional accuracy on the front side after etching completely through a 5- to 10-mil thick silicon wafer.

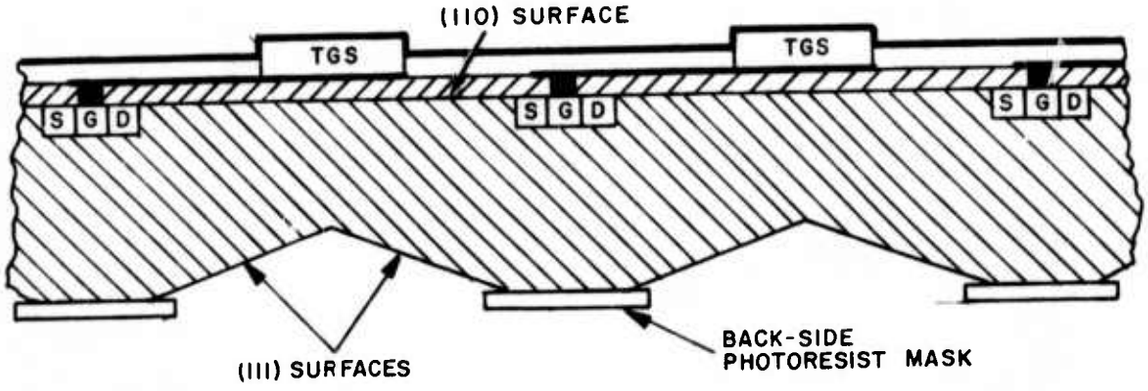
Many alkaline etches for silicon attack (111) crystallographic planes very slowly compared with all other planes.[8] Therefore, the straight-sided surfaces of the etched silicon as shown in Fig. 1-3 are realizable if the silicon wafer and the integrated circuit are initially oriented so that these sides will be (111) planes. However, the silicon crystal has three sets of (111) planes making an angle of 70°32' with each other; during etching, all three sets might be exposed. If one attempts to etch individual holes under each detector as illustrated in Fig. 2-4 (top), one is not only forced to use paralleogram-shaped holes (to have both pairs of sides (111) planes), but also is confronted with the third set of (111) planes that are exposed by the etch as shown in Fig. 2-4 (bottom) that effectively stop the etching before the desired structure is reached.

However, if one considers slots (i.e., long narrow "holes" spanning many detectors as shown in Fig. 2-5), the above problems with extraneous (111) planes largely vanish. The disturbing (111) planes give rise to sloping ends to the slots (as shown in Fig. 2-5), which can be arranged to be outside of the mosaic area proper. The resulting shape of the SiO_2 film at the front (active) side of the wafer is an elongated parallelogram as shown in Fig. 2-6. This figure is a top view photograph of the structure of Fig. 2-5 (but without an integrated circuit or detectors) as viewed in transmitted light. The silicon is opaque and appears dark, whereas the silicon dioxide bridging the slots is transparent and appears light in the picture. Although not obvious in Fig. 2-6, the sides of the silicon bars separating the slots are vertical. However in this early attempt, erratic undercutting of the back-side etch mask and nonplanar sides are evident in the photograph. The following section of this report will discuss the details of the technology that has been developed for producing the uniform and controlled undercutting necessary to produce planar sides of the dimensional accuracy required.

The slots in Fig. 2-6 are approximately 10 mils wide and 0.375 inch long with 4 mil wide bars of silicon between them. It has been observed that silicon bars



a. Top view of TGS detectors arranged over a mosaic of holes etched in silicon.



b. Cross-sectional view showing incomplete etch-through in thick silicon substrates.

Fig. 2-4. Etching of small holes in silicon and its associated problems.

as small as one mil wide (and 8-10 mils deep) are remarkably strong and can withstand unusually rough treatment without breakage. There have been no serious breakage problems associated with the 2 mil wide bars required for the 16- by 16-element array of Fig. 2-3. The silicon dioxide supporting film is another matter because good thermal isolation requires that it be as thin as possible. It has been found that 12,000 Å is about as thin as one can go and hope to have the films survive subsequent processing. TGS layers have been deposited on top of 12,000 Å thick supporting films and then fully processed into undelineated detectors as a demonstration of the feasibility of this approach to the problem of thermal isolation.

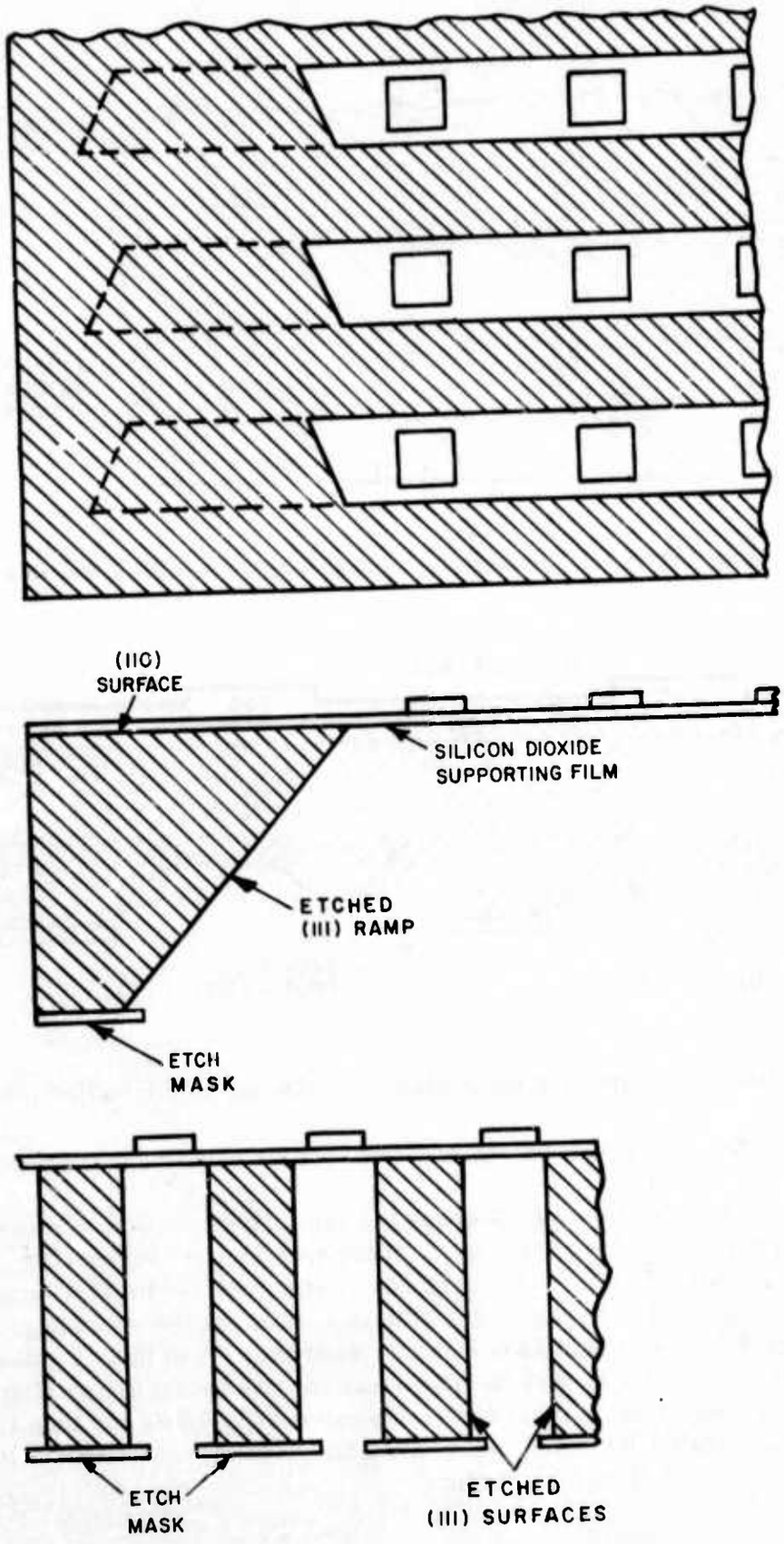


Fig. 2-5. Etching of slots through silicon substrates to achieve thermal isolation.

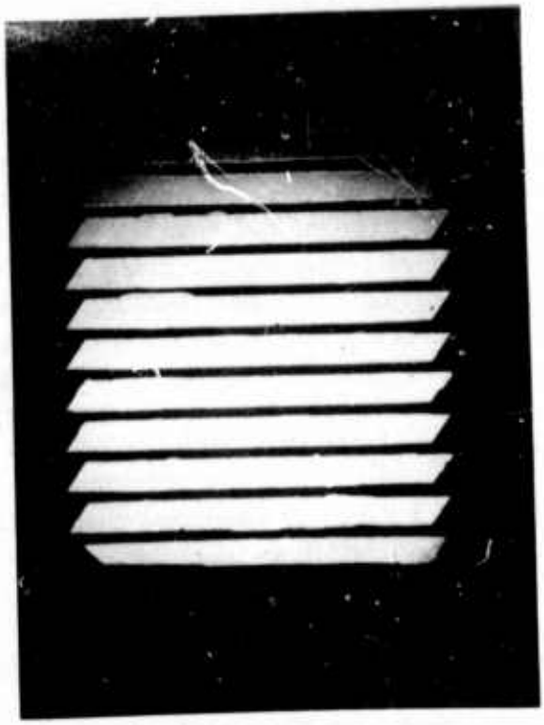


Fig. 2-6. Photograph of silicon dioxide film bridging 10-mil wide slots in an 8-mil thick silicon wafer.

The present technique of thermal isolation has one additional feature worth noting. Nothing must be done before conventional PMOS processing to implement thermal isolation except 1) selection of wafers with the desired crystallographic orientation, 2) initial optical polishing of the back side of the wafer, 3) growing a thermal oxide layer on the back side (to be used later as the etch mask), and 4) providing for the proper alignment of the front-side integrated circuit along a (111) direction. Ordinarily, the back side of a silicon wafer is left with a rough ground finish because it is not critical in any of the fabrication steps. No difficulties arise from it being optically polished and oxide coated. It is only after all standard processing steps are completed (but just before the wafer would be subdivided into individual chips) that etching from the back is initiated. No problems of compatibility have arisen between the present thermal isolation technology and the conventional fabrication processes used in the manufacture of integrated circuits.

The necessity for thermally isolating the mosaic detectors has been demonstrated by simulating the situation with the large area test detectors used to obtain the data of Fig. 2-2. Three separate test detectors were made: one on a 14-mil thick silicon substrate to simulate no thermal isolation, one on a 5-mil thick glass substrate to simulate the detector used in Fig. 2-2, and one on a stretched 1/4-mil thick mylar film to simulate the thermally isolated mosaic detector. The voltage responsivities of these three detectors were measured at various frequencies ranging from about 10 Hz (for typical values pertinent to imaging applications) to 120 Hz. The detector with the silicon substrate exhibited a responsivity at 120 Hz that was about 1/10 of that of either the glass or mylar supported detectors. This clearly demonstrates the large degradation in performance caused by the thermal loading of the high thermal conductivity silicon substrate. The frequency dependence of the measured voltage responsivities of

these three detectors is shown in Figure 2-7. The data have been normalized to a relative responsivity of unity at 120 Hz, for ease of comparison. Notice that the thermally isolated (mylar supported) detector exhibits the expected 1/f dependence and thus has its responsivity improved by a factor of 3-5 as the frequency is reduced from 120 Hz to the 10-30 Hz range of interest for imaging. The detectors constructed on glass and silicon show much less frequency dependence because, as the frequency is lowered, more time is available for thermal conduction, thus increasing the effectiveness of the thermal loading of the substrate. By comparing the data for the detectors mounted on silicon and on mylar, one immediately concludes that failure to provide thermal isolation will result in a loss of voltage responsivity by a factor of from 20 to 30 (depending on the frequency of interest). Therefore, it is quite apparent that thermal isolation will be required in order to achieve the sensitivities one requires for almost any application presently envisioned for infrared imaging mosaics.

3. Improving the Pyroelectric Properties of Polycrystalline TGS

Several techniques for modifying the pyroelectric properties of TGS by altering its crystal structure have been reported. These include:

1. Increasing the Curie temperature and pyroelectric coefficient by deuterating some (or all) of the hydrogen in the glycine component.[9]

2. Lowering the Curie temperature and displacing the hysteresis loop by irradiation of the TGS with X-rays.[10]

3. Increasing the Curie temperature by preparing "alloy" crystals of TGS with the isomorphous compund triglycine fluoroberyllate or lowering the Curie temperature with the compound triglycine selenate.[6,11]

4. Shifting the hysteresis loop completely to one side of the zero electric field line by use of large molecule additives that substitute for glycine in the crystal structure (e.g., ℓ-alanine or sarcosine).[5,12]

The first three techniques are completely compatible with the basic concepts of polycrystalline detectors and could be applied to the starting material. The fourth technique, however, results in a permanent poling of the starting material that precludes the necessary repoling of the randomly oriented grains after deposition of the polycrystalline layers. While this may be a useful technique for single crystal detectors, it is not directly applicable to polycrystalline detectors.

Another possible modification of TGS would be the broadening of the hysteresis loop, i.e., to make the loop more nearly square. The coercive field (E_c) is the field required to switch the polarization. In a square loop the value is abrupt and all switching will occur at a single voltage. In a nonsquare loop (see Fig. 2-8(a)) switching will occur over a range of voltages. The value of coercive field (E_c) is defined as the field present when the polarization is equal to zero.

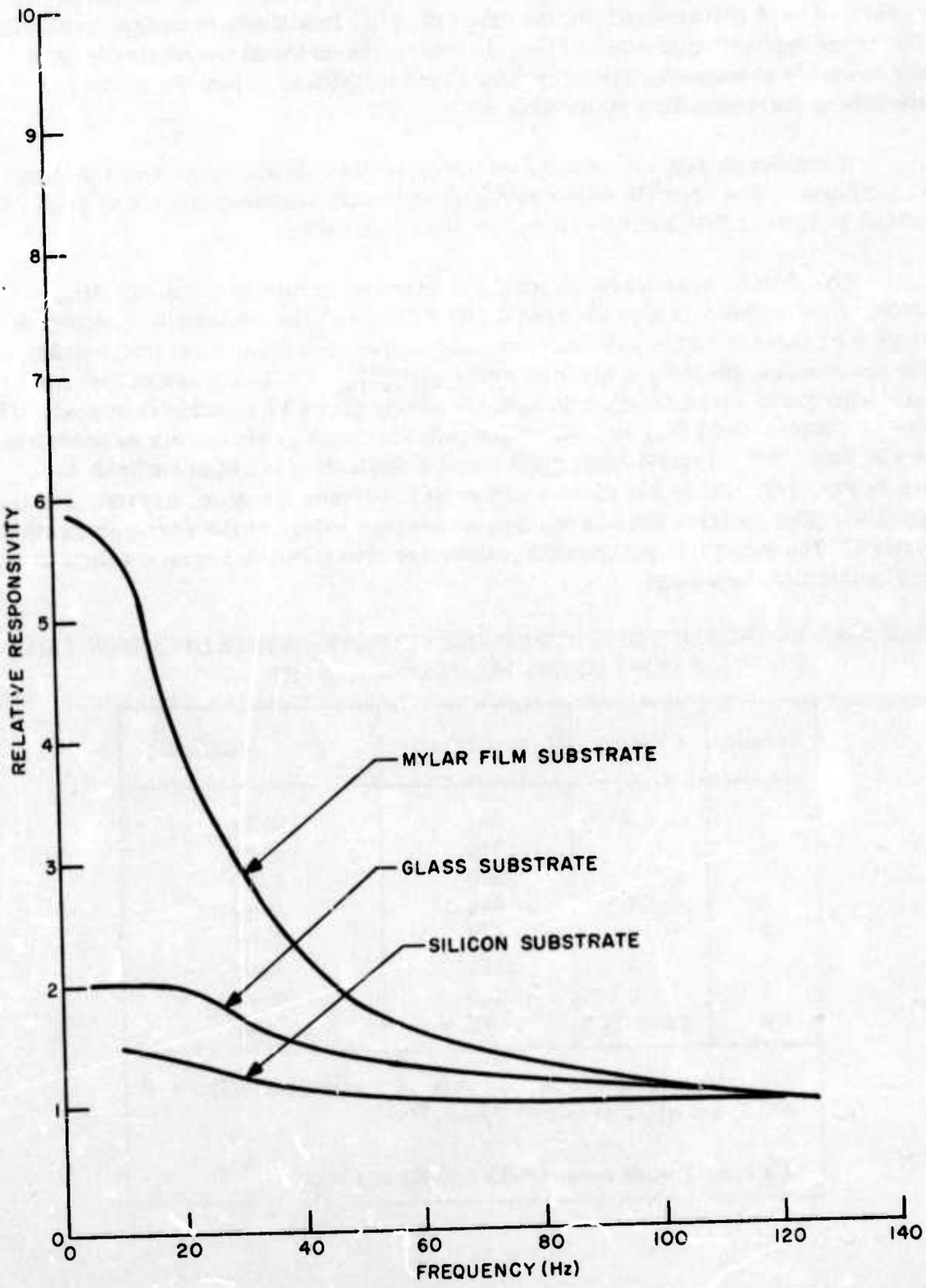


Fig. 2-7. Comparison of the relative frequency response of polycrystalline TGS detectors mounted on various substrates (normalized to unity response at 120 Hz).

Several advantages can be gained from doping to broaden the loop. First, the coercive field is increased and thus the crystal is less likely to depole on standing or under the application of weak fields. Secondly, the material would also be less likely to depole at temperatures below the Curie transition. Also, the method is applicable to polycrystalline materials.

A number of TGS crystals doped with glycolic acid and propionic acid have been examined. The crystals doped with propionic acid exhibited electrical properties identical to those of TGS and so will not be discussed further.

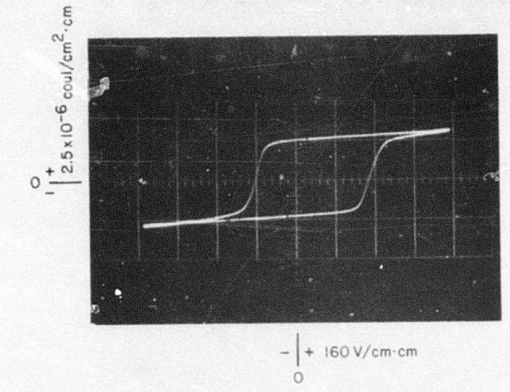
The glycolic acid doped crystals have shown interesting but conflicting results. Five samples of glycolic acid doped TGS have been evaluated. Samples 1 through 4 were cut from two crystals grown by evaporation from a saturated solution of the composition $(\text{glycine}_{0.9}\ \text{glycolic acid}_{0.1})_3H_2SO_4$. Sample 5 was cut from a crystal also grown with 10% glycolic acid but slowly grown by solution transport. The values of coercive field (E_c) and saturation polarization (P_s) for the six samples are shown in Table 2-3. Typical hysteresis loops (polarization vs. applied field) are shown in Fig. 2-8. Table 2-4 gives a comparison between the doped crystals and undoped TGS. The coercive fields are taken as average values at the zero polarization crossings. The saturation polarization values are also taken as average values at the zero electric field crossings.

TABLE 2-3. PROPERTIES OF TRYGLYCINE SULFATE CRYSTALS GROWN FROM SOLUTION CONTAINING 10% GLYCOLIC ACID

Sample	Crystal	E_c (volts/cm)*	P_s (10^{-6} coul/cm^2)
1	1	224	2.50
1	1	720	4.60
2	1	240	2.97
2	1	640	4.69
3	2	810	3.38
4	2	1211	2.69
5	3	155	2.91
6	Pure TGS	72.2	2.04

*Literature values of E_c for pure TGS vary from values of 400 V/cm at 25°C to 220 V/cm.[13,14]

All values were measured at 60 Hz at 25°C.

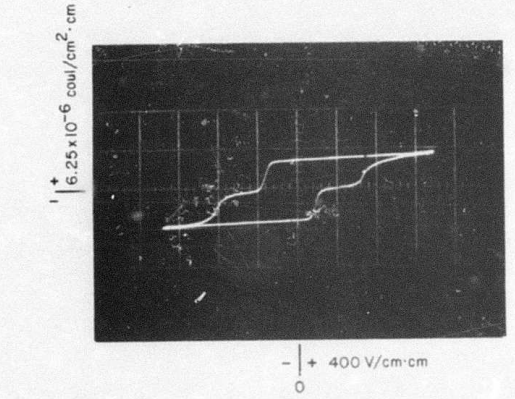


a. Sample No. 1, glycolic acid doped TGS.

E_c avg = 224 V/cm

P_s avg = 2.5×10^{-6} coul/cm^2

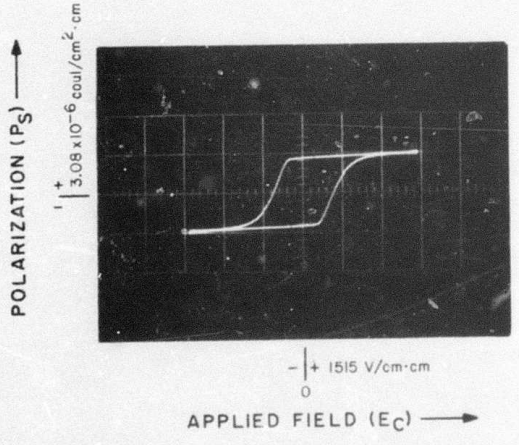
Sample area = 0.02 cm^2
Sample thickness = 0.125 cm



b. Sample No. 1 with higher applied field; the hysteresis loop develops a second component. If the coercive field of this component is considered one finds

E_c avg = 720 V/cm

P_s avg = 4.6×10^{-6} coul/cm^2



c. Sample No. 4, glycolic acid doped TGS.

E_c avg = 1211 V/cm

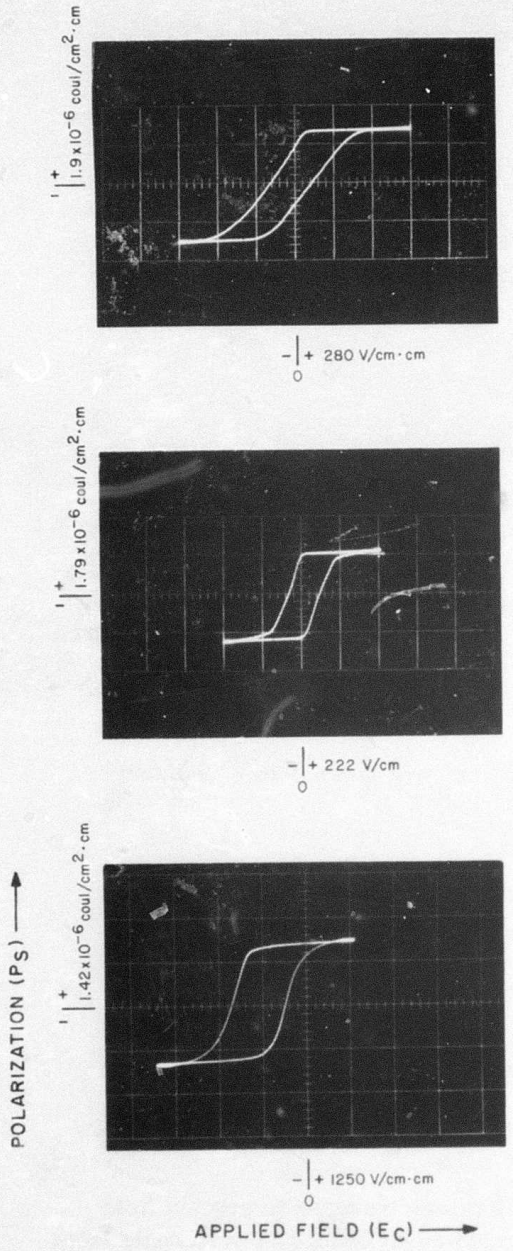
P_s avg = 2.69×10^{-6} coul/cm^2

Further increase in applied field showed no change in hysteresis loop.

Sample area = 1.49×10^{-2} cm2

Sample thickness = 6.6×10^{-3} cm

Fig. 2-8. Hysteresis loops for doped TGS samples (1 of 2).



d. Sample No. 5, glycolic acid doped TGS grown by solution transport.

E_c avg = 155 V/cm

P_s avg = 2.91×10^{-6} coul/cm^2

Specimen area = 0.258 cm^2
Specimen thickness = 0.0356 cm

e. Sample No. 6, undoped TGS

E_c avg = 72.2 V/cm

P_s avg = 2.04 coul/cm^2

Sample area = 0.28 cm^2
Sample thickness = 0.09 cm

f. Sample No. 7, analine doped TGS. Note shift in zero corresponding to an internal bias of 1250 V/cm.

Fig. 2-8. Hysteresis loops for doped TGS samples (2 of 2).

TABLE 2-4. COMPARISON OF PROPERTIES OF GLYCOLIC ACID DOPED CRYSTALS TO TYPICAL UNDOPED TGS CRYSTALS

	E_c (volts/cm)	P_s (10^{-6} coul/cm^2)	Dielectric Constant	Pyroelectric Coefficient (10^{-8} coul/cm^2 °C)
Sample 3 Crystal #2	810	3.38	30	2.35
Sample 5 Crystal #3	154.6	2.91	34	2.50
Typical Data for TGS	100 - 400	2 - 3	30 - 40	2 - 4

The data in Table 2-3 show a large variation in the measured values of E_c. Samples 1 through 4 (grown by evaporation) give values of E_c which are considerably higher than accepted values for TGS. It is known that crystal perfection has an influence on E_c. The less perfect the crystal (higher dislocation and point defect content) the higher the coercive field. Temperature and frequency of measurement will also affect the values obtained. E_c is also dependent on the thickness of the crystal.

For the application in question here, it is necessary that the doped crystals have a true coercive field, i.e., a field E_c below which the crystal will not switch no matter how long a field is applied to the crystal. In order to assure that a ferroelectric has a true coercive field it is necessary that a plot of the natural log of the switching time versus the reciprocal of the applied field (E) tends to infinity as $1/E$ approaches $1/E_c$. Such measurements have yet to be made.

The results obtained from Samples 1 and 2 indicate that the crystal may have been a bicrystal containing two regions of different orientation. Unfortunately this could not be resolved optically due to poor quality of the specimen faces. Samples 3 and 4 showed well-behaved hysteresis loops and indicate a broadening of the loops. However, Sample 5 (Fig. 2-8) shows no loop broadening.

The crystalline quality of Sample 5 was much superior to the other crystals since much more care and time was taken with its growth. In all cases the growth habit of the crystals grown from a solution containing glycolic acid was much different from undoped TGS. Glycolic acid doped crystals do not cleave as TGS and samples must be cut with a string saw. It is not known at present how much glycolic acid is incorporated into the TGS crystal lattice, and an analytical determination of glycolic acid in the crystals would be desirable.

Although it is not possible to ascertain with certainty the effect of glycolic acid on TGS, present indications are that there may be some loop broadening.

B. TECHNIQUES FOR ETCHING THE THERMAL ISOLATION SLOTS

1. Initial Crystallographic Alignment

Since the techniques of etching the thermal isolation slots from the back side of the wafer require photolithographic definition of an etch mask on the back side, it is necessary to polish the backside rather than leaving it rough ground as is done conventionally. In addition, the geometrical arrangement of the three sets of (111) planes illustrated in Fig. 2-5 requires that the wafer surface be a (110) crystallographic plane instead of the more common (100) or (111) planes. The slots must be aligned with respect to the (111) planes and the integrated circuit must be aligned with respect to the slots. Accordingly it is necessary to provide some means of aligning the circuit with respect to the (111) planes that will ultimately define the vertical slot walls. This has been done by first lightly etching a small exploratory area near the edge of the wafer using the (111) plane-revealing etch (to be discussed below). This exploratory area is defined by a randomly oriented square hole in the 5000 Å thick thermally grown SiO_2 mask that otherwise covers the entire wafer. Although the three sets of (111) planes are clearly revealed in the etch pattern, it is not long enough for accurate alignment. Therefore, a long rectangular alignment slot is aligned to the exploratory area as shown in Fig. 2-9 and etched deeply into the silicon wafer. The preferential nature of the etch "overrules" any slight misalignment and most of the resulting slot length is etched to a planar (111) surface. The intersection of this vertical (111) wall with the wafer surface forms a sharp line that can then be used for the initial alignment of the integrated circuit on the wafer.

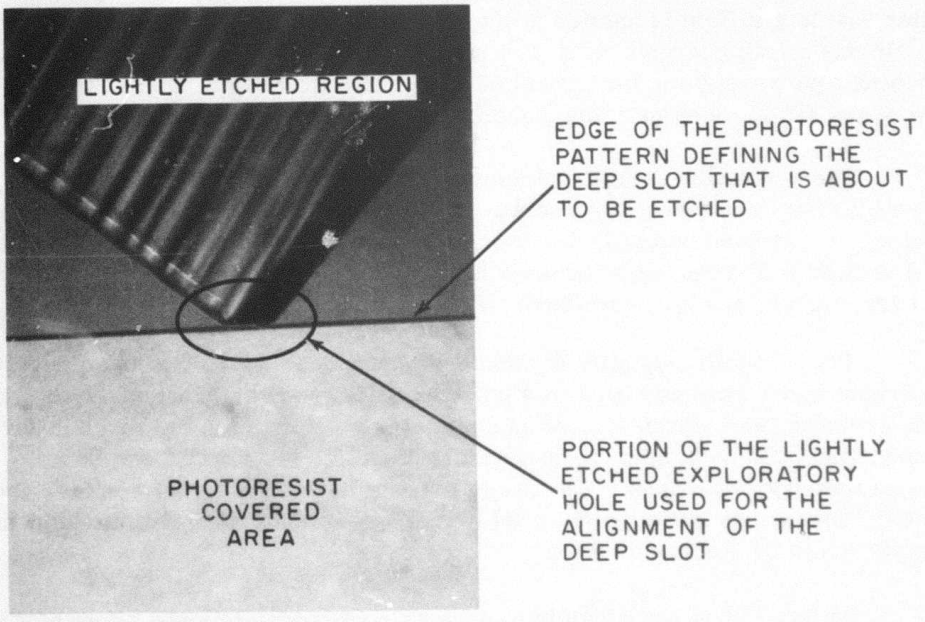


Fig. 2-9. Initial identification of the vertical (111) planes.

At this point, Step 1 of Table 2-1 has been completed and the wafer is ready for conventional processing (Step 2 of Table 2-1). Figures 2-1 and 2-3 are pictures of the active side of the 16- by 16-element bucket-brigade area arrays as returned from PMOS processing and ready for etching of the thermal isolation slots. Table 2-5 summarizes in greater detail what has already been done at this point (I) and what remains to be done (II).

2. Etching the Silicon out from Under the Detectors

The back sides of the wafers of Figs. 2-1 and 2-3 are uniformly coated with a layer of silicon dioxide about 15,000 to 20,000 Å thick that was thermally grown during the various oxidizations of PMOS fabrication and was intentionally left intact. The oxide must now be defined into a series of slot openings to allow the etch to reach those portions of the silicon substrate to be etched away. The alignment of the photoresist exposure mask is done by using an infrared (light) aligner that permits one to "see through" the wafer and directly align the back side slot openings to the existing front side circuitry. After alignment, the slot openings are etched in the silicon dioxide mask as outlined in Step II-A of Table 2-5.

Preferential etching of the silicon wafer through the openings in the back side oxide mask is perhaps the most critical step in this process. The hot KOH-water etch recommended by Stoller[8] and the alcoholic-KOH recommended by Price and Estricher[15] were both found to slowly attack silicon dioxide (i.e., both the mask material and the supporting film that bridges the slots once they become exposed). They both produced erratic undercutting of all etch masking materials investigated. The hydrazine-water etch studied by Lee[16] was superior in both of these respects, but tended to leave a residue in the slots that lead to erratic and incomplete etching. Incorporation of catechol or isopropyl alcohol into the hydrazine etch to act as a complexing (solubilizing) agent as recommended by Lee[16] reduces the already low etch rate to practically zero. The ethylenediamine-catechol-water etch described by Fine and Klein[17] is the best etch found to date and, in fact, leaves little to be desired except speed (its etch rate* at 90°C is about 1-mil per hour in the (110) direction). Figure 2-10 is a photograph of the corner of a 16-by-16 bucket-brigade array that has been provided with slots using this etch. The photograph was taken in transmitted light to clearly show the slots (light areas) against the opaque (dark) silicon background. Notice the opaque lower electrode/pads and the clock lines that are on top of the silicon dioxide film bridging the slots (compare Fig. 2-10 with Fig. 2-3). Although these slots are not perfect, they are much better than those reported earlier[18] and shown in Fig. 2-6 using the alcoholic-KOH etch of Price and Estricher.[15]

All of these basic etches slowly attack the aluminum metallization of the integrated circuit and, therefore, the active side of the integrated circuit must be protected. Although a number of materials were evaluated as protective etch masks

*For a mixture of 25 cc ethylenediamine, 4.5 grams of catechol, and 12 cc of water. This is the composition recommended by Fine and Klein[17] and used for all the results with this etch reported herein.

TABLE 2-5. SUMMARY OF THE SLOT ETCHING TECHNOLOGY

I. Preparative Procedures

A. Select (110) wafers that are optically polished on both sides.

B. Grow a 5000 Å thick thermal oxide on both sides of the wafers.

C. Using this oxide as a masking material, etch a deep alignment slot on one side of each wafer to identify the axis of the future slots.

II. Etching the Thermal Isolation Slots in the Completed Integrated Circuit

A. Definition of the back-side oxide mask:

1. Apply photoresist.
2. Expose photoresist in the infrared aligner.
3. Develop photoresist.
4. Etch the thermal oxide in buffered hydrofluoric acid.
5. Remove the photoresist.

B. Etching of the silicon wafer:

1. Mount the wafer in the etching apparatus of Fig. 2-11.
2. Solvent clean the surface to be etched.
3. Remove any residual oxide on the exposed silicon surfaces by pre-etching in 1% hydrofluoric acid solution for 5 seconds.
4. Etch the silicon with ethylenediamine-catechol-water etch at a temperature of 90°C for 10 hours.
5. Pour off the spent etch and allow the apparatus to cool.
6. Rinse-out the interior of the etch apparatus in water.
7. Dismount the etched wafer from the etching apparatus.

C. Final clean-up:

1. Remove the Apiezon Black Wax in trichloroethylene.
2. Remove any residue remaining in warm photoresist stripper.*
3. Rinse successively in trichloroethylene, acetone, and methanol (taking care not to break the delicate SiO_2 films).
4. Allow to dry without "spinning-off" the residual methanol.

*e.g., Resist Strip J-100 (see Appendix A)

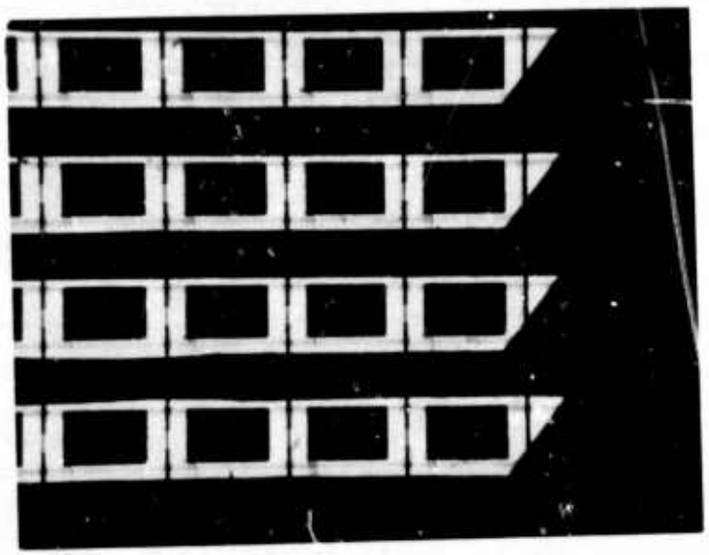


Fig. 2-10. Photograph of thermal isolation slots etched with ethylenediamine-catechol-water etch as seen in transmitted light.

(see Table 2-6), no material was found that would withstand the ethylenediamine-catechol-water etch for the 8-to-10 hours required to etch through a standard 10-mil thick silicon wafer and/or be chemically removable after completion of etching. Mechanical etch confinement proved to be the best technique and an etching jig (Fig. 2-11) was constructed that holds the wafer against the bottom of the etch container in such a way that the etch is constrained (by an "O-ring" seal) from reaching the aluminum integrated circuit metallization. The slots pictured in Fig. 2-10 were made this way, and when this array is viewed by reflected light (see Fig. 2-12), it is seen that the aluminum metallization is still intact. Figure 2-12 also illustrates the tendency of the bridging SiO_2 films to bow outwards due to the fact that the film is initially in compression as a result of differential contraction as the wafer was cooled (during PMOS processing) from the temperature of the oxide growth furnace (typically 1100°C) to room temperature. Figure 2-13 is a closer view of one of the detectors of Fig. 2-12 and shows that despite bowing, everything is intact.

Once exposed, the bridging SiO_2 films are very delicate and easily broken. Therefore, the films are supported during etching by backing the wafer with a thick layer of Apiezon Black Wax*. If the wax is preheated to 200°C for one-half hour it is rigid enough at the 90°C etch temperature to provide the necessary mechanical support required for the films to withstand the hydrostatic pressure differences and/or forces

*See Appendix A for a list of the sources of the materials used in this project.

TABLE 2-6. PROPERTIES OF MASKING MATERIALS (TO WITHSTAND ETHYLENEDIAMINE-CATECHOL-WATER ETCH AT 90°C)

Material*	Maximum Lifetime
I. Photoresists	
1. Kodak KTFR	1 hour
2. RCA Resist	5 minutes
3. GAF PR-115	10 seconds
4. Shipley 1350	10 seconds
II. Waxes and Tars	
1. Asphalt#	10-15 hours
2. Apiezon Black Wax#	2 hours
3. Tar	30 minutes
III. Miscellaneous Materials	
1. Silicon dioxide	Greater than 20 hours
2. G.E. Silicone Resin SR-319	1-5 hours
3. Epoxy resin#	2 hours
4. Gold#	Less than 5 hours
5. G.E. Glyptal 1201 Red Enamel	30 minutes
6. Polyvinylpyrollidone plastic	30 minutes
7. Microstop	15 minutes
8. Collodion	5 minutes
IV. Combination Masks	
1. Glass over G.E. SR-319 Silicone Resin#	Greater than 10 hours
2. Asphalt over G.E. SR-319 Silicone Resin#	Greater than 10 hours
3. Glass over Apiexon Black Wax#	About 10 hours
4. Evaporated gold over G.E. SR-319 Resin	About 2 hours
5. Deposited SiO_2 over Aluminum#	About 2 hours

*See Appendix A for list of manufacturers of these materials.

#These materials were difficult to remove and/or clean-up after etching.

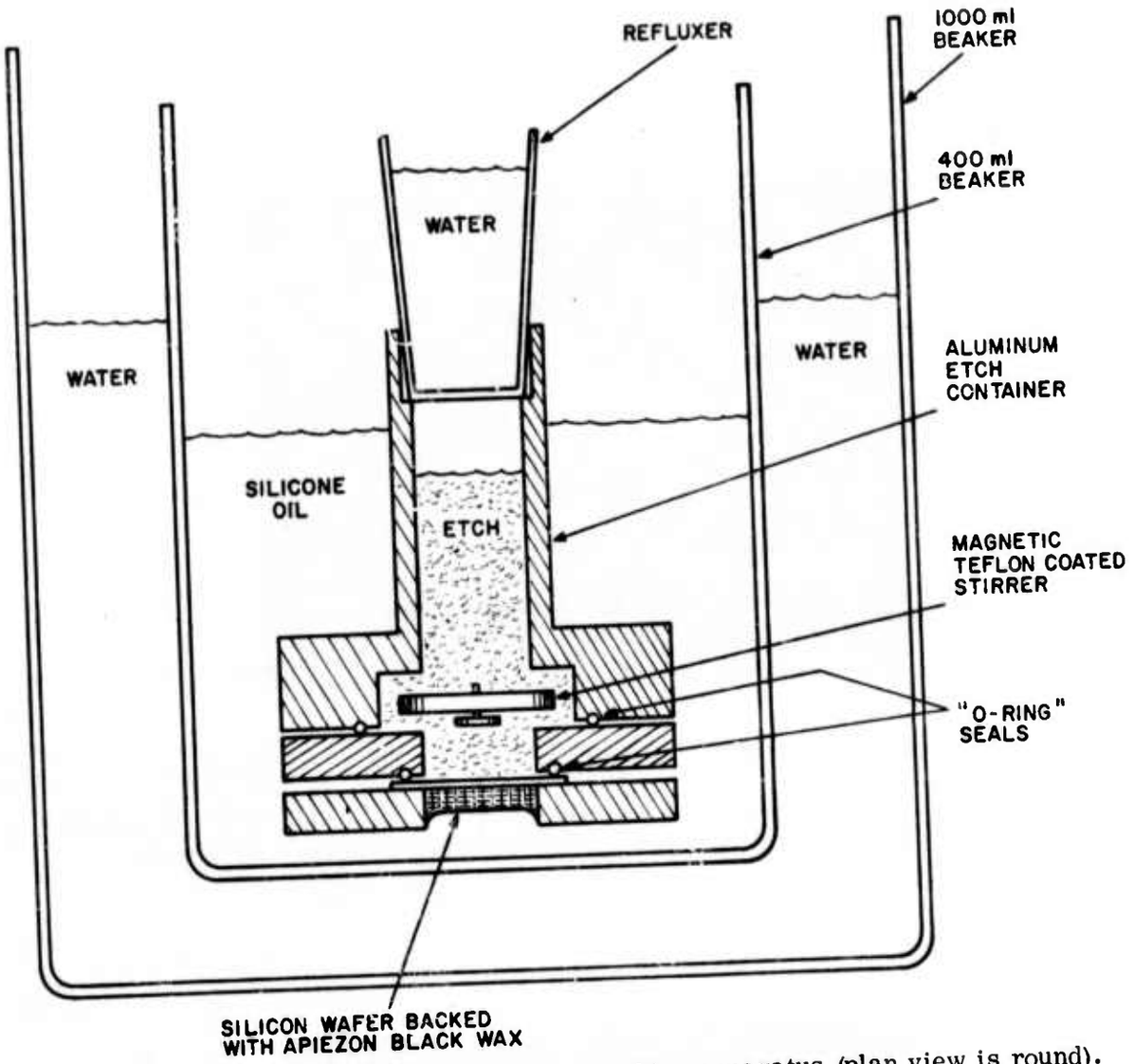


Fig. 2-11. Details of the aluminum etching apparatus (plan view is round).

produced by stirring the etch. The silicone oil surrounding the aluminum etch container serves two purposes. It provides for better thermal communication between the etch container and the intermediate beaker, thus producing the degree of temperature uniformity in the etch bath necessary for uniform etching, and since the etch is immiscible with the silicone oil, any leakage of etch simply "balls-up" and falls harmlessly to the bottom of the beaker.

After completion of the etching, the etch container is withdrawn from the silicone oil and the etch poured off while still hot because a residue forms that is difficult to remove if the etch is allowed to cool while in contact with the wafer. The empty etch jig is then set aside to cool to room temperature. When cool, the etch jig is rinsed in water and the Apiezon Black Wax is removed from the wafer by dissolving

Fig. 2-12. Photograph of the section of array shown in Fig. 2-10 but observed in reflected light to reveal the details of the integrated circuit.

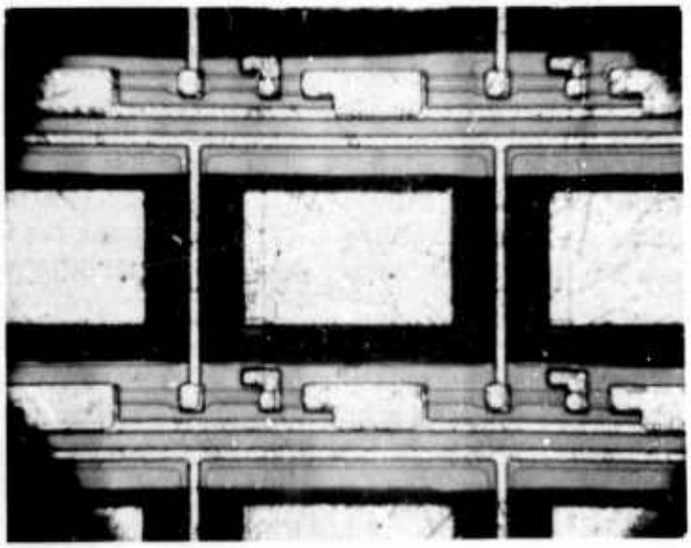


Fig. 2-13. Close-up view of the details of Fig. 2-12.

it in trichloroethylene. If any residue remains on the wafer at this point, it can usually be removed by treatment in warm J-100* followed by successive rinses in trichloroethylene, acetone, and methanol. In any event, the bridging SiO_2 films are very delicate and easily broken and extreme care is required in the post-etch cleaning operations.

Although this process is capable of producing the good results shown in Figs. 2-10, 2-12, and 2-13, the yield of good arrays is still comparatively low. Figure 2-14 is a photograph of another array from the same wafer of Figs. 2-10, 2-12, and 2-13 that illustrates several of the things that can (and often do) go wrong. One additional fault (not visible in Fig. 2-14) is the tendency for an unconnected network of cracks to form in the SiO_2 films. These cracks are attributed to bowing of the films as they are "freed" from the silicon substrate during etching and the initial compressive stress is relieved (see Fig. 2-12). One possible solution to this problem is to use supporting films of silicon oxy-nitride which can be made to have the same thermal expansion coefficient as silicon by suitable adjustment of the oxide-nitride ratio.[19] However, since this would have involved modification of the standard PMOS processing procedures with unknown effects on yield and performance, no attempt was made to implement this idea. Cracks that interrupt circuitry (e.g., the clock lines crossing the slots) ruin the whole row of detectors, but isolated cracks are harmful only in

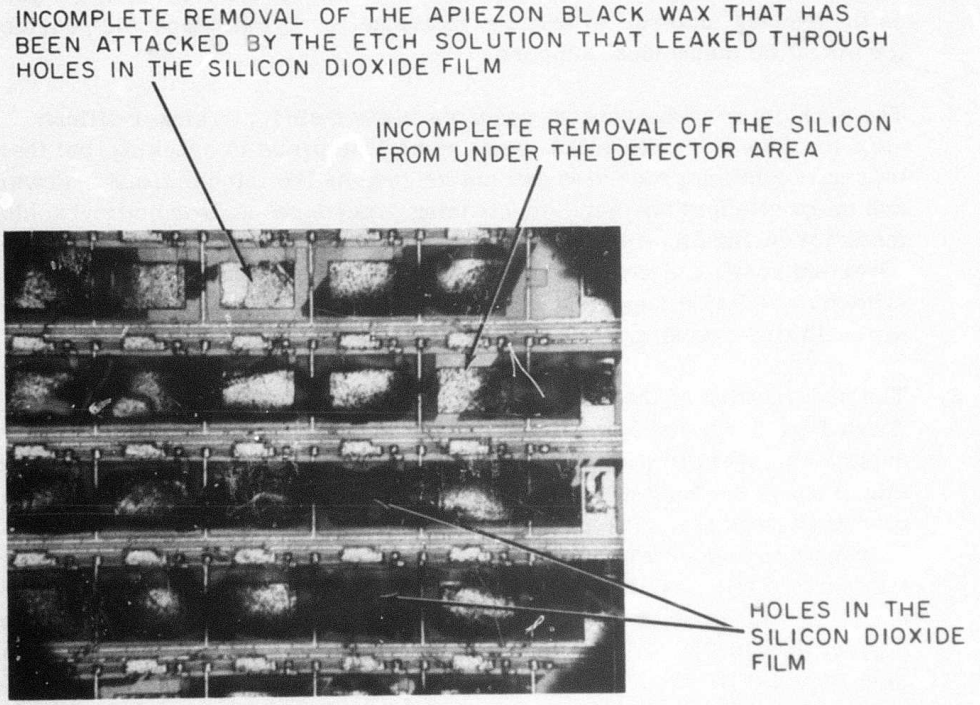


Fig. 2-14. Photograph of an array that illustrates some of the pitfalls in the present etching process.

*See Appendix A.

that they weaken the film and make it more susceptible to breakage. There is sufficient strength in the TGS film, however, that once it is applied there is little danger of breakage unless the wafer is badly mistreated.

3. Additional Technologies Required

Although the present techniques can give good results, the yield is poor. There are a number of areas in which improvements in the technology could be made that would increase the overall yield. These include:

1. A material (that does not soften at the 90°C etching temperature) to replace the Apiezon Black Wax would minimize breakage of the silicon dioxide films during etching. This new material should be easily and completely removable by a single solvent treatment (in spite of having been attacked by the etch leaking through broken or cracked silicon dioxide films). In addition, the material should have a fair degree of resistance to attack by the etch to enable it to continue to perform in the event of breakage or cracking of the silicon dioxide film. If a material satisfying these criteria could be found, it might then be possible to chemically separate the individual arrays from the parent wafer during slot etching and depend on the backing material to hold the individual arrays in place and provide for all of the mechanical support.

2. The problem of film cracking requires further study. Thicker silicon dioxide films (e.g., 20,000 Å) seem to be less prone to cracking, but their thermal isolation properties are not as good as the thinner films. Fewer and more efficient post-etching cleaning procedures and/or better backing material during etching may be helpful in inhibiting cracking due to inadvertent rough handling in processing. Perhaps the feasibility of using silicon oxy-nitride supporting films should be investigated as a technique for inhibiting cracking due to release of compressive stress and bowing.

3. The undercutting of the etch mask during etching has been estimated (from Fig. 2-10) and found to be 0.9-mil of undercutting per 10-mils of slot depth. However, in order to realize this low an undercutting, a very exact alignment of the back-side etch mask to the previously aligned front-side circuit is required. The present techniques are not sufficiently accurate. In some extreme cases, where the misalignment has approached one degree, the entire silicon bar between the slots of Fig. 2-10 has been undercut and etched away. In other cases, where the angular alignment has been more perfect than in Fig. 2-10, the undercutting has been almost negligible (see Fig. 2-15). Notice that the slots of Fig. 2-10 and Fig. 2-15 are slightly off-center with respect to the center-line of the lower electrode pads. This is due to an undetected displacement misalignment in the infrared aligner at the time of exposure of the photoresist to define the back-side silicon dioxide etch mask. This positional misalignment error results from

the fact that it has not been possible to simultaneously focus on the back-side exposure mask and on the front-side circuitry at any but the lowest magnifications of the aligner microscope. This problem arises because the two planes are separated by at least the silicon wafer thickness (i.e. 10 mils) and the depth of field of most microscopes is not this large at the higher magnifications. In the case of Figs. 2-10 and 2-12, the combination of angular and positional errors has yielded acceptable slots whereas in the case of Fig. 2-15, more undercutting and better positional alignment would have been preferred.

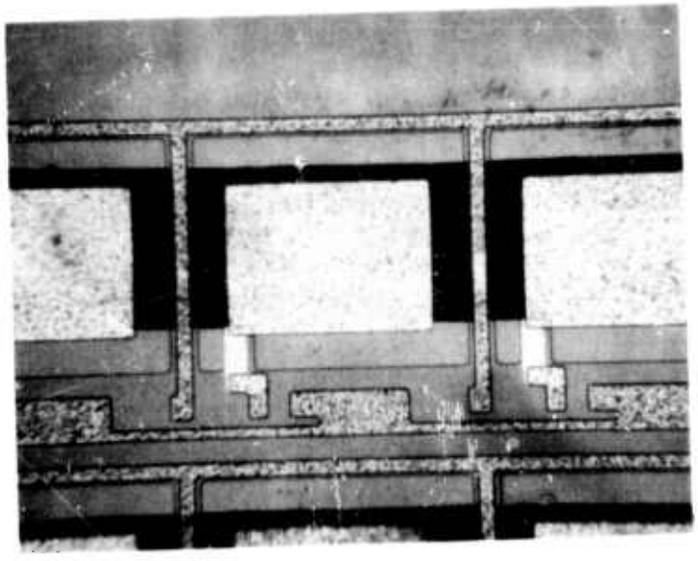


Fig. 2-15. Photograph of a section of an array viewed in reflected light, showing the undesirable effects of positional error of alignment of the slot to the integrated circuit.

It is thought that the major new technologies required for the etching of the thermal isolation slots have been developed (but, perhaps, not fully perfected) to the point where acceptable slots can be produced. However, it has been demonstrated that the present bridging silicon dioxide film technology is, in fact, a viable approach to the problem of thermal isolation and only needs some refinements of existing technology to increase the yield to reasonable levels.

C. TECHNIQUES FOR DEPOSITION AND DELINEATION OF POLYCRYSTALLINE TGS FILMS

Many materials can be prepared in thin film form by vacuum evaporation or sputtering techniques. However, TGS is a delicate organic compound that quickly decomposes below its melting point (233°C)[20] and/or at temperatures at which it exhibits an appreciable vapor pressure. In addition, TGS is a molecular compound composed of glycine and sulfuric acid molecules, neither of which can be readily deposited in situ by chemical reactions. Attempts to prepare TGS films by solvent (water) evaporation techniques have demonstrated the remarkable ability of TGS to grow into large single crystals. The resulting "films" consisted of large (several mm) needle-like crystals on an otherwise bare substrate and were unsuitable for the present purpose. The most successful technique has been to deposit submicron particles of TGS into a film and to provide some means of holding them together. Beerman[3] and Weiner[21] have suggested making films by mixing finely ground TGS with a binder (plastic) to form a paint which may then be applied to a substrate. The binder, however, "dilutes" the pyroelectric properties of the film* and its use may preclude any possibility of delineating the film into small individual detectors by photolithographic masking and etching techniques. These considerations led to the present development of suspension spraying and settling techniques. Both of these techniques have been found to yield good quality films and have been used interchangeably to produce the films and test detectors reported herein.

1. Preparation of TGS Suspensions

The objective in preparing suspensions of TGS for either spraying or settling is to attain a stable** suspension of icron sized particles in some suita inert carrier fluid. Isopropyl alcohol has und to be sufficiently volatile for both the spraying and settling processes. It has sufficient wettability to TGS and the intended substrate materials to prevent surface tension induced "balling-up" of the suspension. However, TGS is slightly soluble in isopropyl alcohol (to the extent of about 0.4 grams/liter at room temperature) and, by so dissolving, introduces the sulfate radical into the suspending medium. The presence of the sulfate radical has been shown to increase the tendency of the individual TGS particles to agglomerate and settle. The most effective way found to inhibit agglomeration is to presaturate the suspending medium with glycine. This reduces the solubility of TGS to almost zero. In fact, the use of glycine presaturated isopropyl alcohol as the suspending medium has been the largest single factor responsible for our success in reproducibly preparing stable** suspensions of TGS.

The most satisfactory method of preparing suspensions of submicron sized particles of TGS has been ball milling a mixture of the component parts for approximately one week. It is necessary to presaturate the isopropyl alcohol with glycine prior

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*Beerman recommends using from 1% to 25% binder (based on the dry weight of TGS).
**Stability is herein defined as no visible settling for several hours to, perhaps, one day.

to the TGS addition and not allow the temperature of the mixture to change (and thus upset the desired saturation conditions) during ball milling. It has been found that even a small amount of contamination introduced during milling is remarkably effective in altering the physical properties of the deposited films. Therefore, a study was made to optimize the milling operation as judged by the attainment of stable suspensions with a minimum of milling time and contamination. The best results were obtained using a ball mill consisting of a 1000-ml polyethylene container partially filled with 125 glass marbles and 300-ml of glycine-saturated isopropyl alcohol, to which 2 grams of TGS are added just prior to milling. After one week of milling, if a stable suspension is not obtained, it can usually be made stable by treating it ultrasonically for a few minutes (but taking care not to heat it in the process). The contamination introduced by this process has been measured to be about 2% glass and 10% plastic (with respect to the dry weight of TGS) in addition to 3% glycine intentionally introduced to achieve suspension stability. Since glycine is soluble in virtually all TGS etches, its presence does not seriously affect the etchability of the resulting films (an important consideration during delineation of the film into individual detectors). The glass and plastic contaminants are another matter and will be discussed below.

In addition to the ball milling process described above, a number of other approaches to obtaining contamination-free TGS of submicron particle size were examined. Commercial tungsten carbide and an alumina grinding mills were both found to be far more contaminating than the plastic mill using glass balls.

TGS was also ground in a jet mill which employs two opposing high speed air jets. The material to be ground is introduced into one of the jets. It then passes through a centrifugal separator and the larger particles are transferred to the second air jet. The larger particles then bombard the incoming material in the first jet. Grinding is thus accomplished by the impact of the TGS particles with each other and should be contamination free. TGS ground by this method has resulted in particle sizes of 3-μm to 5-μm. It should be possible to achieve a smaller particle size by optimizing the operating conditions of the mill and/or by making several passes through the mill.

Precipitation from aqueous solutions was also attempted. A saturated solution of TGS in water was sprayed into isopropyl alcohol which has violently stirred in a blender. After spraying the suspension was allowed to dry, thus producing a fine powder of water-free TGS. The powder was then resuspended in glycine-saturated isopropyl alcohol. This method produced TGS with a particle size ranging from 0.5-μm to 5-μm. Further improvements in technique should produce a reduction in particle size.

The films produced from any of these suspensions are held together partly by the glycine that precipitates out as the suspending medium evaporates, but to a greater extent by other contaminants. The plastic contamination in ball-milled suspensions is easily removed by boiling the as-deposited films in trichloroethylene; the

glass and glycine will suffice to hold the film together if the mechanical action of the boiling trichloroethylene is not too violent. In the experiments designed to reduce the total contamination as much as possible (e.g., with the jet mill mentioned above), the as-deposited films showed virtually no coherence or adhesion to the substrate (glass in this case). In another experiment with intentionally long ball milling times (and thus high glass and plastic contamination levels), the deposited films could hardly be scraped off the glass substrates with a razor blade. For the ball milling schedule outlined above, the film coherence and adhesion to the substrates of current interest are just about adequate for the subsequent processing and further purification is probably not desirable.

2. Suspension Spraying and Settling Techniques

The suspension settling process involves placing the substrate at the bottom of a dish, flooding it with a known (calculated) amount of suspension and setting it aside to allow the suspension to slowly settle and the suspending medium to evaporate to dryness. It is very efficient in the use of suspension, but it is time-consuming. It takes from 12 to 24 hours for complete evaporation of the isopropyl alcohol. The suspension spraying process involves spraying (from a suitable atomizer) the suspension onto a heated (to about 100°C) substrate to immediately volatilize the suspending fluid. In the interests of thickness unformity, it has been found necessary to spray the suspension as a fine mist over an area much larger than the substrate, thus leading to very inefficient utilization of the suspension. However, there is no waiting time as in the case for suspension settling, and the film is immediately ready for further processing once spraying is completed.

Both processes yield fairly uniform films if the starting suspension is reasonably stable. The films, however, are loosely packed and have only 0.25 to 0.5 of bulk density and appear opaque and white to the eye (single crystal TGS has the clear colorless appearance of glass). The films provided from ball milled suspensions are sufficiently well bonded to their substrates to withstand normal handling, but not so well bonded to withstand any appreciable mechanical forces (e.g., rubbing with one's finger). The density and adherence are improved by a densification treatment applied to the film after deposition and complete evaporation of the original suspending medium.

3. Film Densification

The most effective method of film densification found consists of a water vapor (steam) treatment that controllably saturates the film with water and dissolves the surface layers of the TGS (and glycine) particles, thus allowing the resulting loose structure of individual grains to collapse*. TGS is very soluble in water (330 grams/liter at room temperature) and the film can not long be exposed to the steam bath or it will completely dissolve in the entrained water. After collapse, the water is allowed to evaporate and the dissolved TGS (and glycine) will precipitate thus recementing the

*A 2% glass contamination level does not seem to interfere with this densification process, but higher levels have been shown to completely inhibit it.

particles into a coherent film and providing adhesion to the substrate. Our experience indicates that films densified in this way have about 80% of bulk density and are sufficiently coherent and well bonded to the substrate to withstand light rubbing and one's finger without damage. However, there is still sufficient porosity to impart a white semiopaque appearance to the densified film.

There is, nonetheless, a tendency for the collapsed water-soaked films to "ball-up" on the substrate (particularly if it is hydrophobic). This results in cracks and/or pin holes in the finished films that are potential short circuits when the upper electrode is subsequently evaporated on the TGS layer. The tendency to "ball-up" can be minimized by carefully cleaning the substrate prior to deposition (to assure that it is hydrophilic). In addition, it has been found advisable to prepare films in steps of 2 or 3 separate depositions with plastic removal and densification being done after each deposition step.

4. Laser Evaporation of TGS Films

A CO_2 laser has been used to evaporate good quality films of TGS. These films have resistivities in the range of 10^{13} ohm-cm and relative dielectric constants of about 30. A number of samples of TGS have been evaporated on 0.02-cm thick glass plates with bottom and top aluminum electrodes. Freshly evaporated samples, poled at 50 to 168 kV/cm for extended periods of time (ranging up to 16 hr), have been found to be pyroelectric, with pyroelectric coefficients of about 5×10^{-9} coul/cm^2 °C. However, the samples degrade with time. It appears that there is a reaction between the laser evaporated TGS and the aluminum electrode material. Examination of specimens that have been setting for several weeks show definite degradation of the films and electrodes. In some cases the pyroelectric coefficient has dropped to almost zero. A plausible explanation of this phenomena is the presence of free sulfuric acid which is reacting with the electrode material.

The plot of pyroelectric current vs. temperature for laser evaporated TGS is quite different from that of either single crystal TGS or also polycrystalline TGS. Laser evaporated TGS does not exhibit a definite Curie transition. The pyroelectric coefficient increases with increasing temperature and then falls to a value of about twice that of the room temperature coefficient. This value of the pyroelectric coefficient continues to remain relatively constant up to the test limit of 100°C. After cooling and reheating, without poling, the pyroelectric effect has disappeared, as would be expected (i.e., the material has been depoled). When the specimen is repoled again the effect is repeatable with the exception being that the fall in pyroelectric coefficient is now at a slightly lower temperature.

Although future work may eventually circumvent these difficulties it is felt at this time that laser evaporation of TGS is not a practical solution for thin film TGS layers.

5. Delineation of TGS Films into Individual Detector Elements

A photolithographic masking and etching technique has been developed for delineating TGS films into individual detector elements. TGS will neither dissolve in nor react with the common photoresist formulations (see Appendix B) and is so soluble in water that water alone should serve as a suitable etchant. Experimentally it is found that the residual 2% glass contamination from ball milling does not seriously interfere with the etching of the films but is, in part, left behind as a trace residue in the etched-out areas. The addition of a few percent hydrofluoric acid to the etch water helps dissolve this residue, but also introduces the danger of etching the aluminum bonding pads on the integrated circuit substrate.

The conventional masking technique of covering the surface to be etched with a thin film of defined photoresist can not be used. Even if the granular surface of the TGS could be covered with such a photoresist layer, the porosity of the underlying TGS (due to incomplete densification) would absorb the etch from the exposed areas of the pattern and thus be etched-out in spite of the protective photoresist mask. Therefore, it is necessary to first fill the intergrain spaces of the TGS film with photoresist and subsequently to develop it fully out of the areas to be etched away.

The negative acting photoresists* have been found to have two undesirable features when used this way:

1. Scattering of light within the translucent film partially exposes the photoresist in those areas intended to be etched away and it becomes almost impossible to completely develop-out the photoresist from these areas.
2. No way has been found to remove the polymerized photoresist from the unetched areas after delineation while leaving the TGS detectors intact.

Therefore, most of the experimentation has been done with positive acting photoresists** wherein:

1. Scattered light may cause some degree of solubilization of the photoresist in the detector areas, but experimentally, this is found not to be a serious problem.
2. Shipley 1350 and GAF PR-115 photoresists can be easily removed from the the delineated film by immersion in room-temperature trichloroethylene for a few minutes. (See Appendix A)

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*Photoresists that are polymerized (i.e., insolubilized) by the exposing ultraviolet radiation so that the resulting photoresist pattern is the negative of the pattern on the exposure mask.

**Photoresists that are chemically changed (i.e. solubilized) by the exposing ultraviolet radiation so that the resulting photoresist pattern is the same as the opaque pattern on the exposure mask.

Shipley 1350 photoresist is a very deep red color and is so opaque that its exposing radiation will not penetrate 10 μm of permeated TGS film. GAF PR-115 photoresist is visually mueh less opaque and can be exposed to the full permeated film depth by simply using long exposure times (e.g., 15 to 30 minutes instead of the more common 15 to 30 seconds).

The best procedure for delineating porous TGS films consists of the following steps: the TGS film is first flooded with an amount of GAF PR-115 photoresist which was ealeulated (or experimentally determined) to fill the film porosity plus enough to leave several micrometers of photoresist on top of the TGS film when dried. The flooded films are allowed to dry for several hours in air (i.e., without "spinning-off" the excess photoresist), stored 8 hr in vacuum, and finally prebaked at 80° C for several hours. The resulting films are completely dry, relatively transparent (due to diminished light scattering with the intergrain spaces filled with photoresist) and uniform in thiekness except for a rim of thicker photoresist around the edge. This rim is meehanically seraped away prior to exposure to allow the mask to make more intimate contact with the film during photoresist exposure.

After exposure, the photoresist must be developed-out of the areas of the film that are to be ultimately etched away. Unfortunately, eonventional positive photoresist developers are all water-based and aceordingly they can etch the TGS films. Although this is not obviously harmful, it has been observed that those faetors whieh promote effective photoresist removal (long development times, agitation during development, etc.) also tend to produce excessive undercutting of the areas of the film one wishes to retain.

A nonaqueous photoresist developer eonsisting of 1 ml 1,1,3,3-tetramethylguanidine per 30 ml ethylene glycol was found to develop GAF PR-115 photoresist if applied as a spray so as to "wash away" the relatively insoluble reaetion products. After about two minutes of spray developing, the photoresist eould be almost eompletely removed from the areas of the TGS film to be etehed away and not visibly removed from the areas destined to become detectors. Continued spraying, however, starts to remove the TGS film from the exposed areas. After about 5 minutes of spraying, the TGS is eompletely removed from the interdetector areas and the detector areas are untouehed except for about 0.5 mils of undercutting around their edges (see Fig. 2-16). If the defining exposure mask is made appropriately oversized, one will have delineated deteetors of the desired size after spray development and removal of the unexposed photoresist. One fringe benefit of this technique is the complete (meehanieal) removal of the glass contaminant by the spraying action of the developer.

6. Evaporation of the Top Layer Metallization

The lower electrode of each array detector element can be laid down on the substrate prior to the TGS deposition and thus presents no partieular difficulty. The top eleetrode is another matter because it must be deposited on the granular top surface of the delineated TGS detector elements. It must be continuous (i.e., electrically conduetiug), and at the same time thin enough to be semitransparent (i.e., nonreflecting) to the infrared light to be detected.

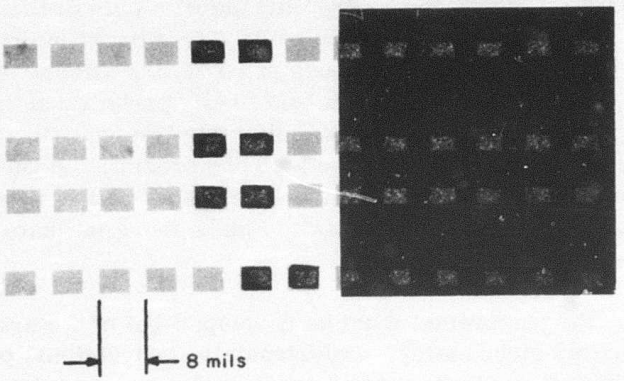


Fig. 2-16. Photograph of the defining exposure mask (left) covering a photograph of the delineated TGS detectors (right). Several cutouts were made in the mask photograph to reveal corresponding TGS detectors.

Metallic films evaporated on the granular top surface of the suspension-based TGS films contain thin spots (e.g., because of shadowing effects of the grains) which dominate in determining their sheet resistance. These thin spots are very susceptible to oxidation and/or migration effects that can cause loss of electrical conductivity. Bismuth metallization has been observed to slowly lose all of its initial conductivity in a few days of air storage. Chromium has been observed to rapidly increase its sheet resistance by a factor of three to infinite resistance when first exposed to air, while aluminum has not exhibited any appreciable oxidization effects. Aluminum, however, has its sheet resistance drastically increased in a few minutes by the passage of large (by the present standards) currents through it.

We have been able, to a large extent, to eliminate these thin spots by simply rotating (or oscillating) the TGS film during metallization so that the evaporated metal arrives at varying angles of incidence, thus filling in the shadows. This technique has produced semitransparent films of aluminum that have sheet resistances atop TGS that are within a factor to two of those simultaneously deposited on glass, whereas without rotation, there would have been a difference of from one to two orders of magnitude (see Fig. 2-17).

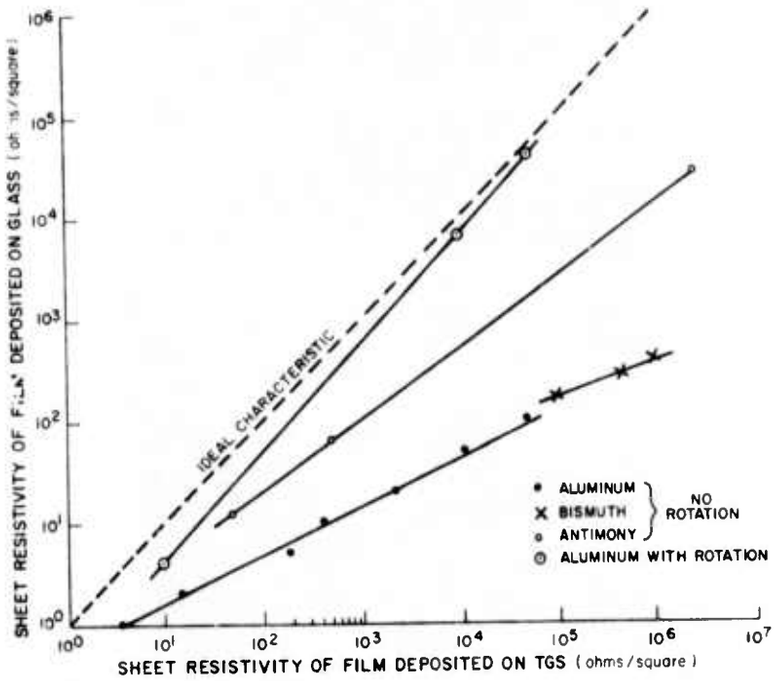


Fig. 2-17. Sheet resistivity of various metallic films deposited simultaneously on glass and TGS substrates.

Figure 2-18 is a photograph of the apparatus which was built to oscillate the TGS layer during metallization. The holder used to support the TGS and a glass monitor slide are shown at the top of the picture in a tilted position. During metallization, a motor continually oscillates the holder through a wide angle about the normal. The oscillation frequency (about 1.5 Hz) is high enough that there are many oscillations in the time required to evaporate the upper electrode.

Electrical shorting between the upper and lower electrodes was a common failure mechanism in early detectors. At first shorting could be traced to pinholes and/or cracks in the TGS films. Later, when the films were improved to eliminate these defects, shorts appeared during poling or just after top layer metallization. It was determined that shorting during poling arose from migration of the chromium electrode material away from the positive electrode, into the TGS layer. Once this was recognized, it was demonstrated that it did not occur when aluminum electrodes were used. Since the use of chromium must be avoided, it may be desirable to select a replacement metal (or alloy) with a very low thermal conductivity in the interest of lowering the heat loss via the contacts and thus improving the thermal isolation of the individual detectors. Although aluminum may not be the ultimate choice of contact material, it has proven quite satisfactory for test detectors designed for TGS film evaluation purposes.

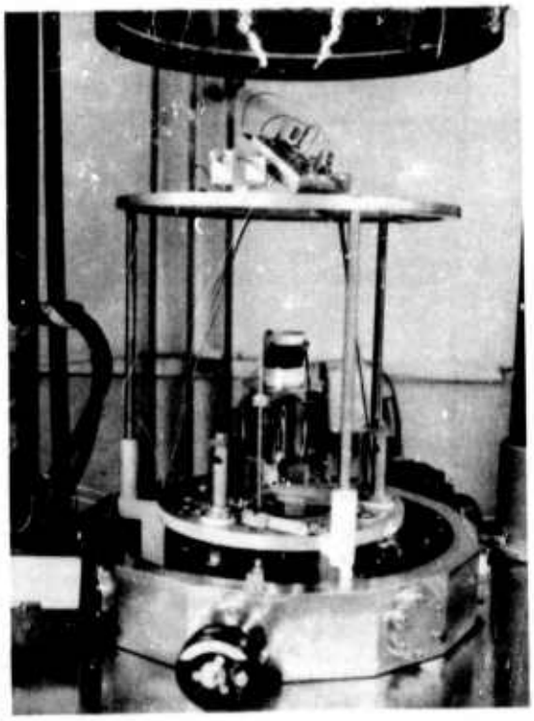


Fig. 2-18. Photograph of the substrate oscillating mechanism used to circumvent shadowing effects during metallization of the TGS top surface.

Experiments with such low thermal conductance materials as bismuth, antimony, cadmium, and their alloys have shown that these materials exhibit poor adherence to substrates and are susceptible to oxidation. The present recommendation is to use a double aluminum metallization technique in which the electrodes per se (including that portion which goes over the edge of the individual detectors) is as thick as necessary to achieve continuity, but the portion transversing the (relatively smooth) thermally isolating silicon dioxide film is relatively thin. This concept has been implemented in our current designs for the lower electrode, but not for the top layer metallization.

7. Additional Technologies Required

Although the present metallization techniques give good results with large area test detectors (e.g., see Fig. 2-17), they have not yet been tested on small delineated detector elements. There is a potential problem in maintaining the continuity of the metallization over the top edge of the delineated TGS detector elements, down the side, and across the (bare) substrate to the next detector. Experiments on evaporation over the edges of large-area mechanically defined test detectors indicate that substrate rotation, necessitated by the rough top surface, will be of considerable aid in accomplishing this task also. It is concluded that the series resistance of the top layer

metallization introduced by going over the edge of the individual detectors will probably not be a serious limitation if connections are provided to the underlying circuitry between each detector and not just at the ends of each row of detectors as implied in Fig. 2-4. In the present bucket brigade area array design (see Section IV) there is a clock line crossing the silicon dioxide supporting film between each detector that has been stripped of its protective silicon dioxide covering so as to permit contact to the top layer metallization as it crosses in its run between detectors.

No attempt has been made to delineate TGS films that were deposited on top of the thin supporting silicon dioxide films of the thermal isolation structure of Fig. 2-5. If the mechanical action of spray developing proves to be too severe for the delicate bridging silicon dioxide films, it will be necessary to stop spraying while there is still an appreciable TGS film (but, hopefully, no photoresist) remaining in the areas to be etched out. In this way, the undelineated TGS film will serve to strengthen the silicon dioxide films during spraying and will then be removed nonmechanically by simply etching in water or water-HF mixtures.

In addition, no attempt has been made to dice the silicon wafers into individual chips containing one (or more) arrays. Conventionally, this is done by scribing and cleaving along the natural cleavage planes of the silicon crystal. However, in the present case, the crystallographic orientation requirements of etching the thermal isolation slots and the delicate nature of the bridging silicon dioxide films probably preclude any kind of mechanical separation procedure. One possible alternative is to chemically separate the individual chips at the time of etching the thermal isolation slots. The price paid for this rather simple solution being the fact that the remaining processing (i.e., from TGS deposition on) must then be done on an individual chip basis instead of being done to all chips simultaneously on a wafer basis.

Section III

SINGLE CRYSTAL PYROELECTRIC ARRAY

The approach to a pyroelectric sensor array described thus far, using a deposited polycrystalline material, has the merit of being compatible with integrated circuit techniques but also involves many problems which have proved difficult to overcome. The alternative approach described in this section uses an unorthodox method of thermal isolation. It allows the use of single crystal material, which has greater sensitivity than polycrystalline material, and also does not require any further etch processes after the integrated circuit elements are formed.

The configuration employed is indicated in Fig. 3-1. The sheet of sensor pyroelectric material is a thin single crystal slab which is spaced a small distance from the addressing integrated circuit array. Contact is made between the FET (field effect transistor) gates in the addressing array and metal pads on the pyroelectric layer by thin metal springs, the thermal conduction of the springs being low enough that they do not act as strong heat sinks. A merit of the system is that the material may be permanently polarized before assembly, thus avoiding the need to apply large voltages after connection to the FET gate. The contact between the pads and springs is not critical since any resistance less than about 10^{10} ohms is enough to discharge the sensor element.

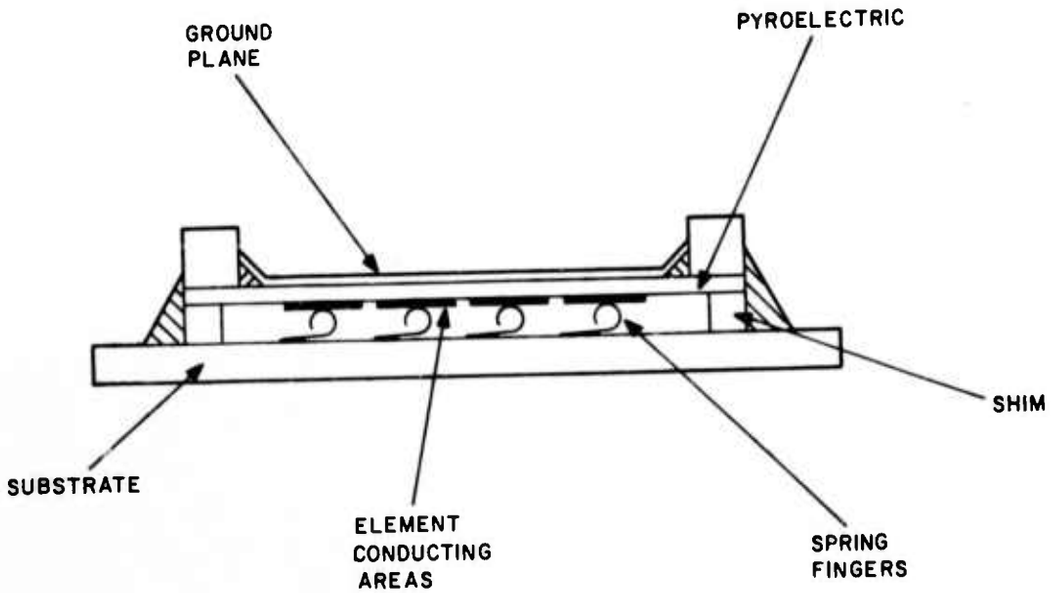


Fig. 3-1. Schematic section of sensor array with thermally isolating finger contacts.

A. THEORETICAL CONSIDERATIONS

1. Heat Sinking

There are two heat loss paths from the pyroelectric layer: through the metal spring fingers and through the ambient atmosphere. Radiative loss is negligible compared with that along these paths. If the dimensions are as follows;

Area of element	$A = 1.6 \times 10^{-4}$ cm^2
Thickness of pyroelectric	$d_1 = 10$ μm
Gap between pyroelectric and substrate	$d_2 = 50$ μm
Cross section area of finger	$A_2 = 2 \times 10^{-8}$ cm^2
Total free length of finger	$L = 10^{-2}$ cm
Thermal conductivity of finger	$k_1 = 3$ watt cm^{-1} °K^{-1}
Thermal conductivity of air	$k_2 = 2.4 \times 10^{-4}$ watt cm^{-1} °K^{-1}
Volume heat capacity of pyroelectric	$C_v = 2.5$ joule cm^{-3} °K^{-1},

then the thermal conductance of the metal finger and air path in series may be calculated. The thermal time constant (τ_T) is the ratio of the heat capacity of the element to the total thermal conductance, i.e.,

$$\tau_T = \frac{C_v d_1}{k_1 A_2/AL + k_2/d_2} \tag{3-1}$$

With the values listed above, which are for 5-mil element spacing, τ_T is 0.03 second. A thicker pyroelectric element would increase τ_T but would also reduce the capacitance and thus increase the signal loss due to the shunting effect of the FET input capacitance. With the above dimensions, the conduction of heat along the finger is approximately equal to the air conduction.

If the frame period is τ_f, that is, if the element is exposed to the source for τ_f and then shuttered for τ_f, then a simple analysis shows that the temperature excursion of the element is

$$\Delta T_d = \left(\frac{W\tau_f}{2Ac_1 d_1}\right)\left(\frac{2\tau_T}{\tau_f}\right) \tanh\left(\frac{\tau_f}{2\tau_T}\right) \tag{3-2}$$

where W is the incident energy per unit area when the shutter is open. The first factor is the temperature excursion in the absence of heat sinking and the remaining factors represent the reduction due to heat sinking. For $\tau_T = 0.03$ s and $\tau_f = 1/30$ s, the reduction factor is 0.02; a structure of the dimensions given above will have very good thermal isolation at this frame rate.

A number of methods of increasing τ_T can be envisaged: thinning the fingers, increasing the air gap, or evacuating the region, but these all bring increasing technological problems for only small signal increases. There is a considerable advantage in maintaining the thermal constant at close to the frame time, in that the thermal history of the target is not retained and smearing of the image of moving objects will not occur.

2. Spatial Resolution

Spatial resolution in this system is limited by lateral thermal diffusion. Calculations have been made of the resolution limit for a bar pattern imaged on a uniform sheet of sensor material; the details are given in Appendix C. The limiting line-pair resolution, i.e. that at which the signal contract falls to half of that occurring in the absence of thermal diffusion, is

$$d_p = 2.9 \sqrt{D\tau} \qquad (3\text{-}3)$$

where D is the thermal diffusivity and τ is the shutter-open time, half the total thermal cycle time. Note that this limit is independent of the thickness of the sensor sheet. For $\tau = 1/30$ s and $D = 5 \times 10^{-3}$ cm^2 s^{-1}, as for TGS (triglycine sulfate), d_p is 3.5×10^{-2} cm (13.8 mils). All the available information in the image can be obtained if three elements are contained in this line-pair spacing, giving an optimum element spacing of 5 mils.

B. FINGER CONTACT ARRAY FABRICATION

Fabrication of the finger contact spring electrodes is effected as follows. First, Shipley photoresist* is laid down over the substrate, leaving clear areas where the ends of the springs are to be attached. Metal fingers are then evaporated through a suitable mask in the sequence chromium, gold, chromium, the thicknesses being approximately 50 Å, 1000 Å and 300 Å, respectively. Finally, the photoresist is dissolved away in acetone. When this is done, the greater tension in the Cr as compared with the Au should cause the fingers to curl to the desired radius.

Evaporations have been carried out using masks with fingers spaced on 10-mil centers, both in 4-by-4 and 16-by-16 arrays. The fingers are 1.5-mil wide by 10-mils long. The mask was fabricated by evaporating a gold film about 5-μm thick onto a 10-mil thick glass square, forming the apertures in the gold by standard photoresist techniques, and then dissolving away the glass under the area of the fingers. It was

*See Appendix A.

found that build-up of metal after many evaporations did not destroy the mask, although there was some curling of the edges of the finger apertures. During evaporation, the substrate is attached to an aluminum plate which has a previously cooled block resting on top to prevent the substrate temperature from rising to the point where the photoresist softens.

More than one hundred evaporations have been carried out using the approximate thicknesses of chromium and gold indicated above. Most were on a glass substrate; a few were on silicon integrated circuit arrays. Figure 3-2 shows the appearance in an interference microscope of the fingers immediately after evaporation through the metal mask onto the photoresist islands, the separation of the interference fringes representing a thickness of 0.295 μm. The islands have gradually sloping rather than sharp boundaries; this effect was achieved by separating the photomask from the resist when the original exposure was made so that the edges became slightly blurred.

The best result obtained after dissolving the photoresist appears in Fig. 3-3. A spiral curl of the correct radius is seen uniformly over most of the array; this form is eminently suited to make low-conductivity contacts of the type desired. Figure 3-4 shows a scanning electron micrograph of one of the fingers. The fingers proved to be remarkably elastic, withstanding compression until they bent almost double without permanent change of shape.

The results of the evaporation shown in Fig. 3-3, which was carried out very early in the series, have unfortunately proved very difficult to reproduce. This particular evaporation was not completely monitored, so it was necessary to cover a fairly wide range of conditions if the original set were to be covered. The usual outcome of an evaporation has been a helical rather than spiral form for the fingers as in Fig. 3-5. Evaporations on silicon integrated circuits also produced this form (Fig. 3-6). A large number of factors may affect the manner and degree of curling of the fingers, more than normally encountered in integrated circuit technology. Some of these are listed in the first column in Table 3-1. The rate and pressure of gold evaporation are probably less important than the other factors. In the later evaporations, all factors in Table 3-1 were carefully monitored. Care was taken to bake the photoresist hard, 10 min at 90° C being the preferred treatment. The range of values covered during different evaporations is given in the second column of the Table. The final column shows a preferred combination of parameters for which several evaporations were made, to check the repeatability. It was here that the difficulty of this particular process became apparent. Of seven evaporations having parameter values close to these, only two gave similar fingers, these having helical curls which although not of the desired spiral form were possibly useful. The remaining five evaporations gave varied results.

One key factor is believed to be the purity of the chromium evaporation filament, which consisted of chromium electroplated onto a tungsten wire. The filament used in the evaporation of Fig. 3-3 was of a kind specially produced to be of high purity

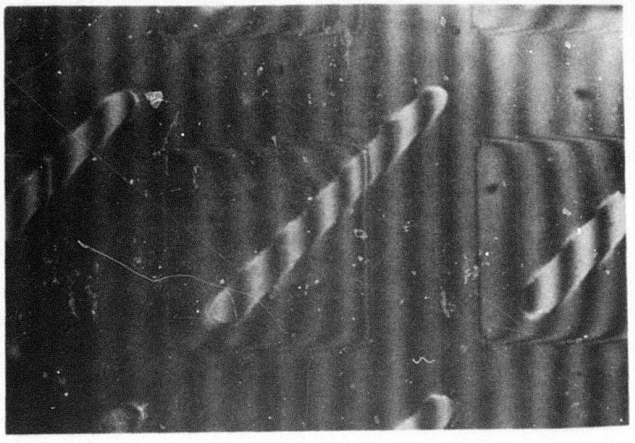


Fig. 3-2. Fingers on glass substrate before removal of photoresist.

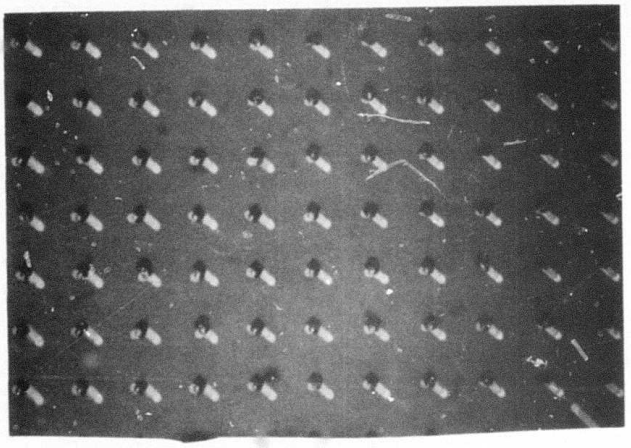


Fig. 3-3. Successfully curled fingers on 10-mil centers on glass substrate.

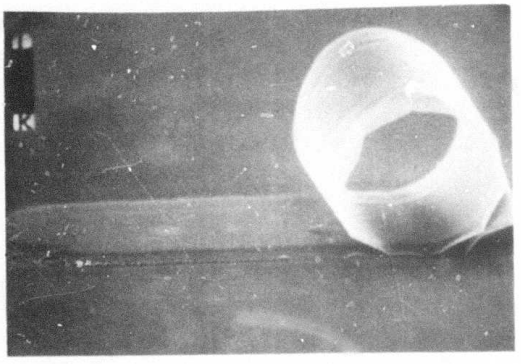


Fig. 3-4. Scanning electron micrograph of successfully curled finger-1000X.

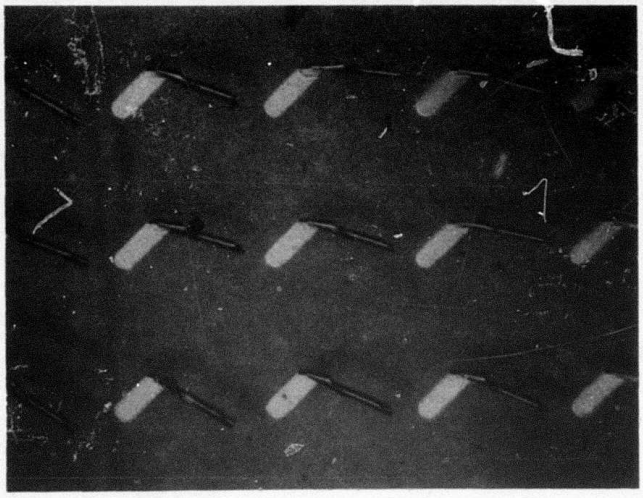


Fig. 3-5. Fingers on glass substrate showing unsatisfactory helical curl.

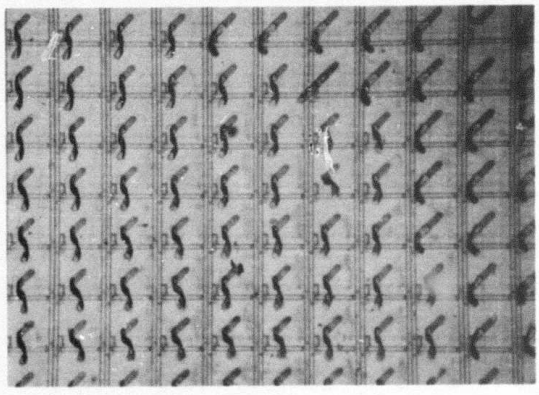


Fig. 3-6. Fingers on silicon integrated circuit.

and was no longer available for the later evaporations. Analyses of the impurity content of filaments from various sources showed the principal impurities to be oxygen and sulfur, the concentrations of these being shown in Table 3-2. There appeared to be a tendency for the more pure filaments to give better results, but the scatter

TABLE 3-1. CONDITIONS OF FINGER EVAPORATION

Parameter		Range of Values Tried	Initial Aim
Cr evaporation rate	Å/second	7 - 35	25
Cr evaporation pressure	$x10^{-5}$ torr	0.4 - 9.0	<1.0
Cr thickness	Å	200 - 500	250
Au evaporation rate	Å/second	15 - 40	30
Au evaporation pressure	$x10^{-5}$ torr	0.7 - 9.0	<2.0
Au thickness	Å	800 - 1500	1000
Photoresist thickness	μm	0.4 - 1.0	0.4
Final substrate temperature	°C	30 - 60	30

TABLE 3-2. ANALYSES OF Cr FILAMENTS USED IN EVAPORATION OF METAL FINGERS

Filament Origin	Wt % Oxygen	Wt % Sulfur
Sylvania (1)	0.15	0.023
Sylvania (2)	0.25	0.01
Mathis	0.39	0.03
(3)	0.025	0.002
(4)	0.28	<0.001

(1) As received

(2) Annealed in hydrogen

(3) High-purity available only for initial evaporations

(4) Heavy plating, origin unknown

is too great for valid conclusions to be drawn. Filaments tended to vary in their manner of evaporation, sometimes evaporating uniformly and sometimes developing hot spots. Several evaporations were also carried out with the substrate tilted at an angle of about 45°, but these gave results similar to those obtained with normal incidence.

C. IMAGING BY ARRAY ELEMENTS

To test the performance of individual elements of an array connected by fingers, a smaller 4-by-4 assembly has been made on a glass substrate with individual connections to the elements. Figure 3-7 shows the substrate and connections with the fingers, and Fig. 3-8 shows the superposed sheet of TGS with the island electrodes mounted in a metal frame. The TGS is 1 mil thick and the islands are on 10-mil

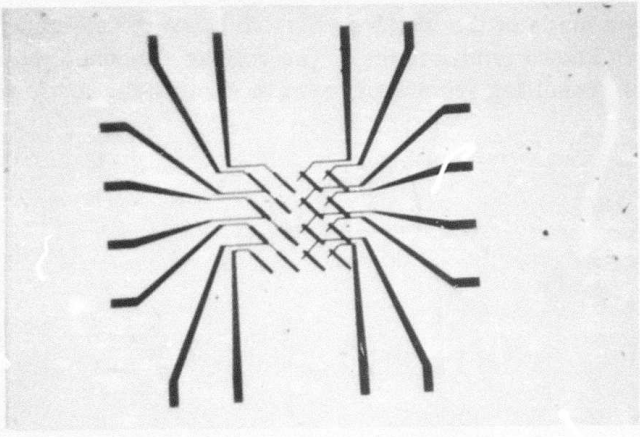


Fig. 3-7. Fingers on fan-out connector strips before photoresist removal.

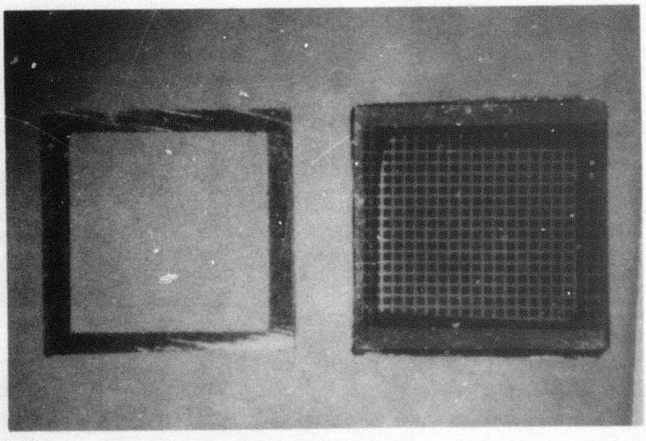


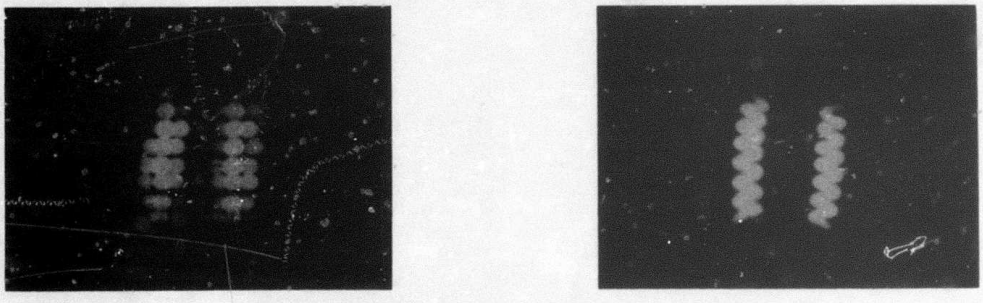
Fig. 3-8. TGS (triglycine sulfate) sheet mounted on frame with island electrodes before mounting on contacts of Fig. 3-7.

centers. A polymer shim 2 mils thick separates the TGS from the substrate and the assembly is held together by a fillet of epoxy resin. Addressing of the array is simulated by mounting it upon a mechanical traverse and moving it by successive 10-mil steps across an image of an infrared source, while the final image is formed by moving a spot on a CRT face by similar steps, the spot intensity being modulated by the output from the pyroelectric element. A test of this kind will demonstrate the spatial resolution that can be obtained with the system.

Figure 3-9(a) shows the infrared image formed by mechanically stepping the single element, while an optical image of the source appears in Fig. 3-9(b). The thermal image was formed by an arsenic disulfide single-element lens and chopped at 15 Hz. The spatial resolution of the thermal image is, as expected, as good as the detector element size.

A test has also been made of the absolute sensitivity of the element by exposing it to a blackbody source of known temperature. The voltage response (peak-to-peak) of the triangular waveform resulting from square-wave excitation, for a wafer with small heat loss, is given by:

$$V = \left(\frac{\frac{dP}{dT}\tau}{2c_v \epsilon} \right) (W/A) \qquad (3\text{-}4)$$



(a) Infrared image (b) Optical image

Fig. 3-9. Infrared image of filament, synthesized by moving element of array by 10-mil steps, and optical image of the same filament.

where

W = incident power into each element

A = area of element

$\frac{dP}{dT}$ = pyroelectric coefficient

c_v = volume specific heat

ϵ = permittivity

τ = shutter open time

If the source is a blackbody at 500° K with a 1.25-cm diameter opening 5 cm from the array, and the shutter open time is 1/30 second, the steady-state voltage output into a high impedance has the theoretical value of 240 mV.

This voltage will be less in practice, due to heat sinking and also to the shunting effect of the amplifier input capacitance C_o which will reduce the voltage by a factor $1/(1 + C_o d/A\epsilon)$. Measurements of the response of the elements used to form the image in Fig. 3-9 gave the rather low value of 6 mV for the signal produced by a blackbody at 500° K with a 1/2-inch diameter aperture at 5 cm distance, the frame time being 1/30 second. This deviation from the theoretically expected value is largely due to the shunt capacitance; however, there remains a factor of about 3 which cannot be readily explained. It is possible that the ground plane on the front face of the TGS is more reflective than the optimum.

In conclusion, it is apparent that the metal finger approach to producing a pyroelectric array is valid in principle. In practice, a reliable procedure to fabricate a large array of fingers has not been developed within the period of this contract, due to the large number of variables in the process which must be optimized. A pair of metals other than chromium and gold might give a broader range of conditions for satisfactory deposition, but substantial further exploratory work is clearly required to demonstrate this.

Section IV

DETECTOR ARRAY ARRANGEMENTS AND SIGNAL READOUT TECHNIQUES

The pyroelectric detectors to be used in the thermal imaging arrays would be fabricated in the form of minute capacitors. Accordingly, it is necessary to sense the signal voltage from each detector of the array with a high impedance element having minimum shunt capacitance. The small detector capacitance also dictates that the sensing element associated with each detector be located as closely as possible to the detector to avoid unwanted lead capacitance. The requirements for high input impedance and low input and lead capacitance are readily met through the use of metal-oxide-semiconductor field effect transistor (MOS-FET) integrated circuits. These circuits are used in both types of two-dimensional pyroelectric/integrated circuit arrays investigated in this program. In the X-Y addressed array, the FETs serve as switched buffer amplifiers which sample the signal voltage generated by the pyroelectric detectors. In the bucket brigade (BB) array, the FETs serve as switching elements which transfer the signal charge from one pyroelectric capacitor to the other. In both the X-Y and BB image arrays, the image sensor portion consists of a mosaic of thin TGS (triglycine sulfate) detectors equally spaced in two dimensions.

A. X-Y ADDRESSED ARRAY

1. Circuit Layout of the X-Y Addressed Array

A schematic of the X-Y addressed array is shown in Fig. 4-1. Each sensor cell contains a thin film TGS detector and two PMOS (p-channel metal-oxide-semiconductor) enhancement mode FETs (a signal FET and a reference FET). One electrode of the detector is connected to the gate of the signal FET while the gate of the reference FET is connected to a common line. All pairs of FETs have their sources connected to their respective column address lines, and their drains connected to their respective signal lines and reference lines. The signal and reference lines are connected to pairs of matched load resistors located external to the array, and the outputs of the FETs appear as voltages across the load resistors. The signals from each row of sensor cells are sensed in a difference amplifier also located external to the array.

Operation is as follows: the gates of the FETs are initially biased at ground potential. The gate of the reference FET is tied to a common ground bus while the gate of the signal FET is biased at ground potential through the resistance of the detector.

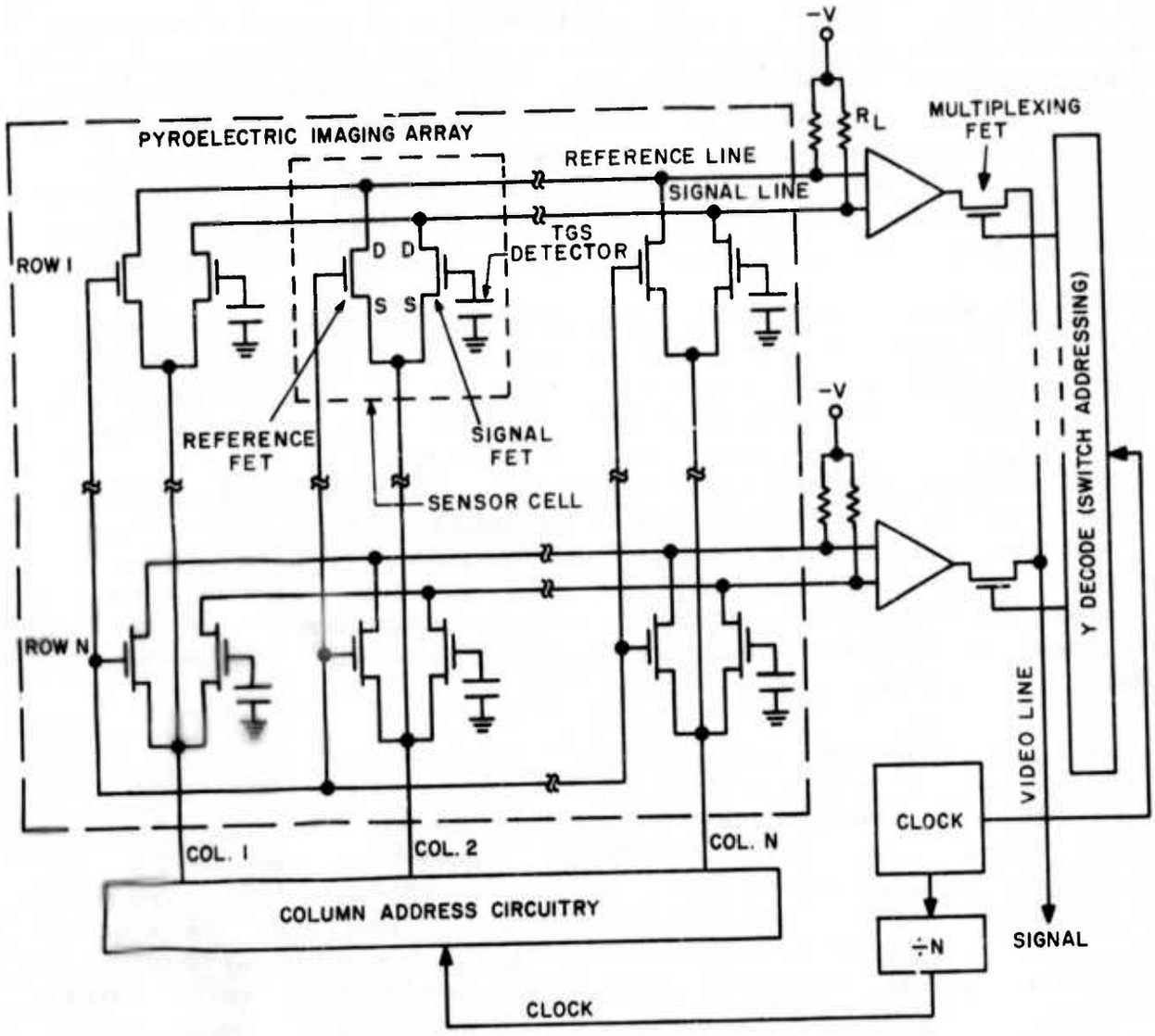


Fig. 4-1. Schematic of an X-Y addressed pyroelectric sensor array, with block diagrams of the addressing and multiplexing circuitry.

Two FETs are used per sensor cell and a difference amplifier is used for each row of sensor cells in order to cancel the unmodulated outputs of the signal FETs, i.e., the pulse amplitudes from the signal FETs that occur even in the absence of a pyroelectric signal. The pyroelectric signal component can be many orders of magnitude smaller than the unmodulated FET output. However, since each reference FET produces virtually the same unmodulated output as its companion signal FET, a difference amplifier can be used to cancel the unmodulated FET components.

Following exposure to the scene, which would occur by means of a continuous motion shutter, the shuttered column line is pulsed positive, creating a negative gate-to-source potential which biases each FET in the addressed column into saturation (i.e., into conduction). The signal and reference FET output voltages that appear across the pairs of matched load resistors are sensed by the differential amplifiers and multiplexed sequentially onto the video output line by the multiplexing FETs. The addressed column is then returned to ground potential, the adjacent column is pulsed positive and the sequence is repeated as each column of detectors becomes covered by the shutter.

The duration of the column address pulse is t_{ex}/N, where N is the number of columns in the array and t_{ex} is the exposure period. The ON period of each of the multiplexing FETs is t_{ex}/N^2, assuming an N-by-N array and equal exposure and shuttered periods, but the bandwidth of the preamplifiers need only extend to N/t_{ex}.

In the X-Y addressed mode of operation, switching transients are introduced by capacitive coupling of the edges of the address pulses through the array crossover capacitances. However, the transients can only be significant on the first row of multiplexed outputs because they die away during the time required to gate out the remaining rows. Additionally, by proper clocking of the multiplexing FETs, the transients—even on the first row—can be allowed to die away before coupling the signal on the video line.

2. Signal Variations

In a system such as the X-Y addressed array, signal variations and fixed pattern noise (FPN) can result. These effects arise from two sources: 1) differences in signal FET transconductances (g_m) across the array, and 2) localized parameter variations between the signal and reference FETs within a sensor cell. The latter results in FPN, the former in a signal gradation for a uniform scene. Estimates based upon parameter measurements of similar FET devices on large scale integrated devices predict that the average variation in g_m will be 1.5%, with maximum variation across the entire array of 6%; neither of these effects is large enough to produce appreciable picture degradation.

Parameter variations within a sensor cell are manifested primarily as threshold voltage differences. These in turn inhibit complete dc cancellation by differential sensing, produce fixed pattern noise, and limit the array sensitivity. The output signal is given by

$$v_o = A_V R g_m v_s \qquad (4-1)$$

where

A_V = amplifier gain

R = drain load resistance

g_m = transconductance of signal FET

v_s = detector voltage

Taking into account localized threshold variations, the output takes the form

$$v_o = A_V R g_m (v_s + \delta V_T) \tag{4-2}$$

where δV_T is the average threshold difference and limits the minimum detectable signal v_s. δV_T results from variations in the density of surface trapping states in the FET gate areas and for devices of the size used in the 16-by-16 array manifests itself in a 1-mV voltage. However, δV_T and its effects can be eliminated by frame storage and subtraction.

3. Address Circuitry and Difference Preamplifier

The address pulse circuitry is illustrated in Fig. 4-2. The circuitry employs active feedback to equalize pulse amplitudes, reducing the common mode requirements of the differential preamplifiers. The amplitude of each pulse is fed back in unity gain fashion to the driving operational amplifier referenced to the desired potential. Switch selection is generated by a "serial in-parallel out" shift register. A single pulse is applied to the input of the register and is sequentially clocked to subsequent outputs of the register. A system utilizing only the register is used to address the multiplexing switches. It is possible to fabricate the column address circuitry on the array. It probably is not practical to attempt to fabricate the differential amplifiers on the chip, although it might be practical to multiplex the rows prior to differential sensing so that only two signal output leads will be required.

A typical design for the difference preamplifier is shown in Fig. 4-3. With the values shown, this amplifier has 10-dB gain and a common mode rejection ratio of 72 dB. Gain can be increased by increasing resistors R_1 and R_2 at the expense of common mode rejection (due to the high source impedance), but the common mode rejection is more than adequate.

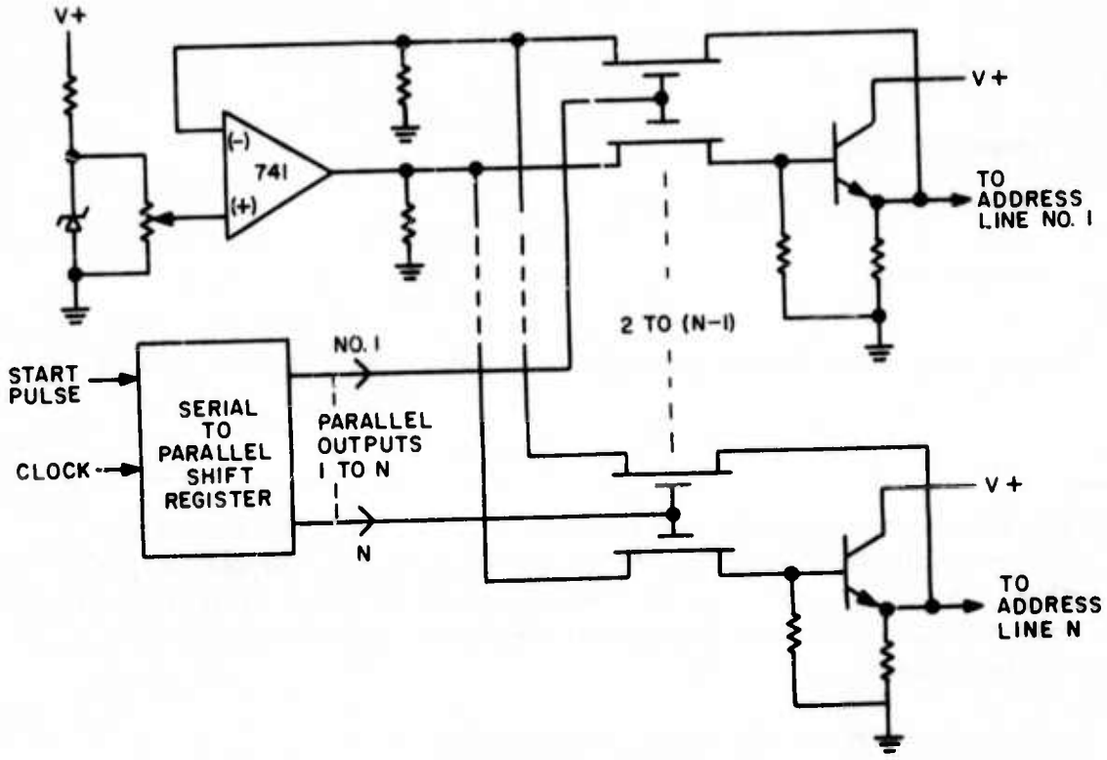


Fig. 4-2. Schematic of column address circuitry.

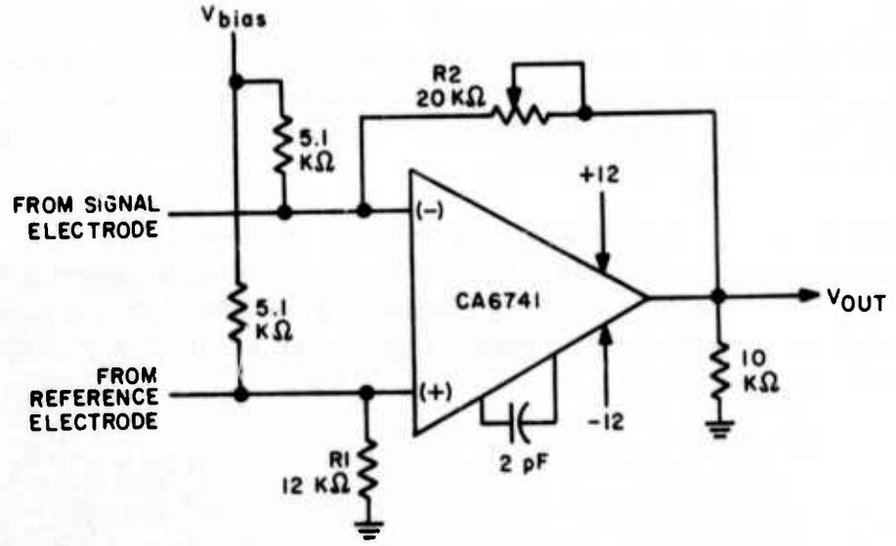


Fig. 4-3. Differential preamplifier circuit.

4. Noise Model for the X-Y Addressed Array

The noise model employed for the detector-FET combination is shown in Fig. 4-4. The gate referred noise voltage (v_{ng}) of the FET,[22] assumed to be all 1/f components, is given by

$$v_{ng}^2/B = \frac{Q}{ZL\omega} \tag{4-3}$$

The noise voltage generated by the passive elements (v_{nJ}) is

$$v_{nJ}^2/B = 4\,kT\,R_c\,(Z') \tag{4-4}$$

where

B = the requisite bandwidth

Q = a parameter containing processing variables, intrinsic silicon characteristics, energy states, and other factors

ω = radian frequency

k = Boltzmann's constant

T = temperature

Z' = complex impedance

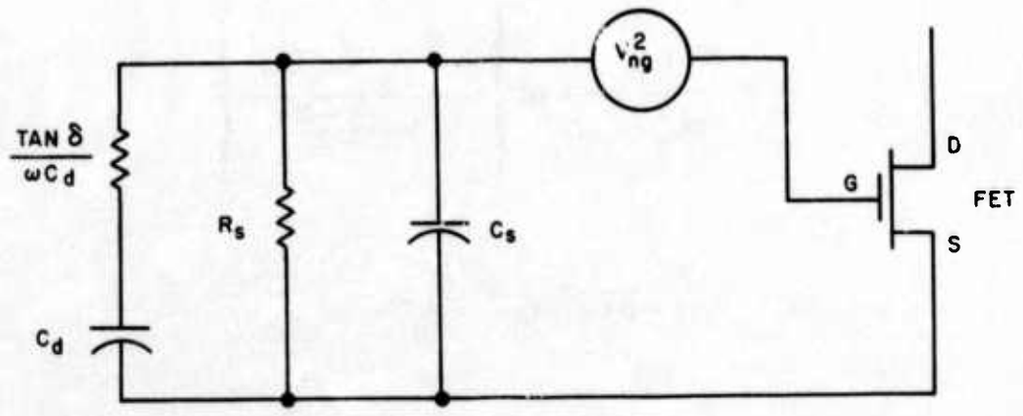


Fig. 4-4. Detector-FET Combination noise model.

The total noise is the sum of v_{ng}^2 and v_n^2

$$\frac{V_n^2}{B} = \frac{V_{ng}^2}{B} + \frac{V_{nJ}^2}{B} \tag{4-5}$$

Total noise over the system bandwidth is found by integrating over the frequency range

$$v_n^2 = \int_{f_1}^{f_2} \frac{v_{nJ}^2}{B}\, df + \int_{i_3}^{f_2} \frac{v_{ng}^2}{B}\, df \tag{4-6}$$

Different limits must be imposed on the two integrals as different noise mechanisms exist. The noise generated by the FET is present only during conduction and the mechanism is presumed to be reset when the device is cut off. This sets the lower limit f_3 at one-half the frame rate F. The upper limit f_2 is equal to the maximum signal frequency attainable on one output line, i.e. 0.5 NF. (N is the number of elements in one row; the integrals were actually extended to NF.) Noise mechanisms on the detector are omnipresent, and since it is employed in a sampled system, the lower frequency limit must be extended to zero. Thus f_1 and f_2 are zero and NF respectively. Upon performing the integration,

$$v_n^2 = \frac{Q}{2\pi ZL} \ln 2N + kT \left\{ \frac{1 - \frac{C_d^2}{C_T^2} \tan\delta}{1 + \overline{\tan\delta}^2 C_a + C_d} \right\}$$

$$+ \frac{kT\, C_d}{\pi C_T^2} \tan\delta \ln \left\{ \frac{4\pi^2 F^2 N^2 R_s^2 C_T^2}{1 + \overline{\tan\delta}^2} \right\} \tag{4-7}$$

where

$$C_T^2 = (1 + \overline{\tan\delta}^2)\, C_a^2 + C_d^2 + 2C_a C_d \tag{4-8}$$

with

$\tan\delta$ = loss tangent of the detector capacitor

C_d = detector capacitance

R_d = detector shunt resistance

C_a = FET shunting capacitance

C_o = FET gate capacitance/unit area

If one assumes tan δ to be small compared with 1, the signal to noise ratio can be optimized by adjusting the FET channel area. This parameter is the one over which there is most control in circuit design. The signal voltage to noise voltage ratio (S/N) is

$$S/N = \frac{v'_s C_d}{C_d + ZLC_o} \Big/ \sqrt{\frac{kT}{C_d + ZLC_o} + \frac{Q \ln 2N}{2\pi ZL}} \qquad (4\text{-}9)$$

and

$$S/N_{opt} = \frac{C_d v'_s}{\left[kT + \frac{C_o Q \ln 2N}{\pi} + 2\sqrt{C_o kT + \frac{C_o^2 Q \ln 2N}{2\pi}}\sqrt{Q \ln 2N}\right]^{1/2}} \qquad (4\text{-}10)$$

where v'_s is the signal voltage generated by the detector with no shunting capacitance. Equation (4-10) shows that S/N increases with detector capacitance and with decreasing surface state density (implied in Q) and has been used to design the FETs for the X-Y addressed arrays analyzed in Section V.

5. Poling the Detectors

Poling the detectors must be accomplished through the series impedance of the signal FET gate. With the array as originally conceived, without individually defined detectors, this was feasible because detector and gate capacitances were comparable and there was sufficient leakage in the contiguous TGS film. Poling of detectors on an array of this type was demonstrated, though uniformity was not determined since the responsivity was very low due to thermal sinking. Defining the detectors, however, increases the gate shunt resistance to detector shunt resistance ratio to 10^4, making dc poling in a delineated X-Y addressed array impossible. Dynamic poling is also impractical since the time constants involved are on the order of 10^4 seconds (measured). Dynamic poling of simulated detector-gate units was accomplished, but it is improbable that this could be accomplished uniformly over a delineated array.

B. PYROELECTRIC BUCKET BRIGADE SENSOR ARRAYS

A bucket brigade register is a device for transferring or delaying analog signals.[23,24] Two modes of operation are possible. The signals may be introduced serially at one end of the register and transferred to the output end, or they may be introduced in parallel at the different storage locations of the array and shifted out serially The latter mode of operation can be utilized to form a two-dimensional pyroelectric sensor array. A partial schematic of a bucket brigade register is illustrated in Fig. 4-5. Operation is such that when the clock line labeled ϕ_1 is pulsed, transistors T_1, T_3, and T_5 are biased into saturation, acting as source follower amplifiers with capacitive loads supplied by the capacitors labeled C_2. The C_2 capacitors are charged to a reset potential, with the amount of charge required being supplied by the C_1 capacitors. The analog signal that is transferred in the register (from left to right in Fig. 4-5) consists of variations in the potential across the C_1 capacitors. Clock ϕ_1 then goes off and the line labeled ϕ_2 is pulsed, repeating the above sequence with alternate transistors (labeled T_2 and T_4) and capacitors, thereby shifting the charge variation one more step along the register. The potential of the last capacitor in the register is sampled, yielding the output signal, or the drain of the last transistor may be tied to a resistor and the charging current monitored.

1. Two-Dimensional Pyroelectric Bucket Brigade Imaging Array

A pyroelectric bucket brigade array can be made, utilizing the circuit of Fig. 4-5, by replacing the capacitors labeled C_1 with pyroelectric detector elements having the same capacitance. The temperature-induced change in detector charge during exposure to the infrared scene can be transferred out of the array in much less time than the detector electrical leakage time constant. A two-dimensional pyroelectric bucket brigade thermal imaging array, composed of N linear bucket brigade registers, each register having N detector elements, is illustrated in Fig. 4-6. The

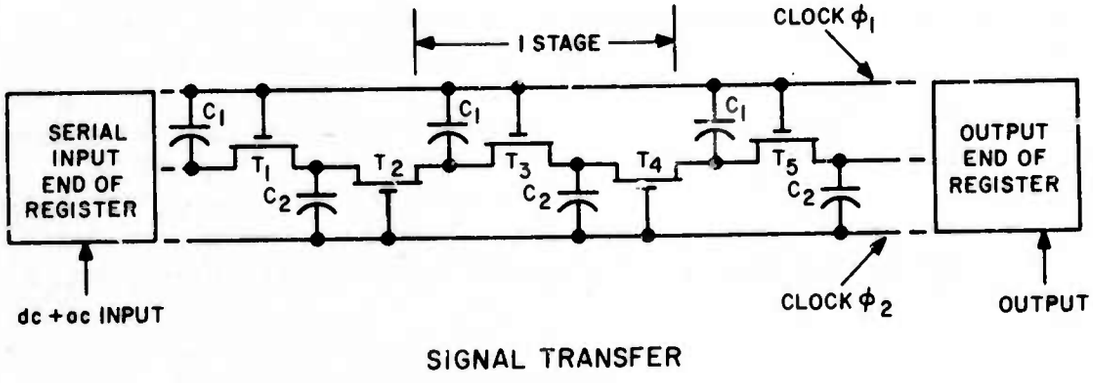


Fig. 4-5. Partial schematic of MOS bucket brigade register.

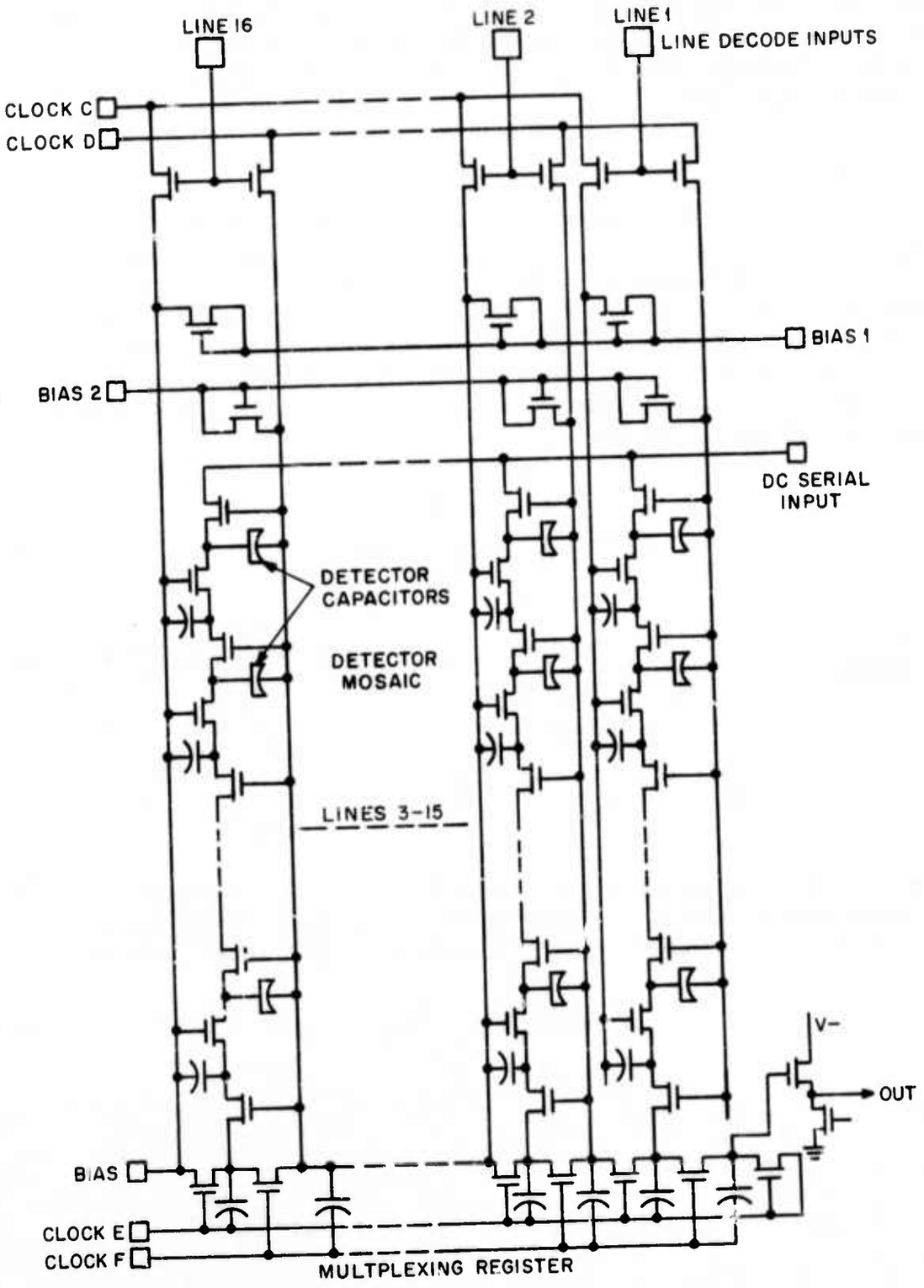


Fig. 4-6. Schematic of 16-by-16 bucket brigade area array.

clocks are gated to one register at a time, allowing total readout of each linear register. Clock gating is performed sequentially, register to register, until the entire array has been scanned. The register outputs are routed onto a multiplexing bucket-brigade register which has the same electrical parameters as the sensing registers. At the end of the multiplexing register there is a buffer FET which samples the signal voltage on the last storage capacitor.

2. Noise

Several noise mechanisms are pertinent for a BB scanned detector array. These include the Johnson noise of the detector itself, the noise introduced during signal transfer (scanning) and the noise due to the output buffer FET. Consider first the detector Johnson noise. The detector is reset to a reference potential once each frame time; this minimizes the effects of low-frequency noise components. Since the noise frequency spectrum is flat, the effect of low frequency noise can be expected to follow an f/f_o dependence for components less than $f = f_o = F_R/4$ where F_R is the frame rate. Detector Johnson noise is simply

$$V_{nJ}^2 = 4kT \int_{f_1}^{f_2} \mathrm{Re}(Z)\,df. \tag{4-11}$$

In light of the above discussion the integral is broken into two parts. The resulting expression is

$$V_{nJ}^2 = 4kT\left[\int_O^{F_R/4} \frac{f}{F_R/4}\,\mathrm{Re}\,(Z)\,df + \int_{F_R/4}^{\infty} \mathrm{Re}\,(Z)\,df\right] \tag{4-12}$$

The upper limit of the second integral is taken to infinity for convenience as the added noise contribution is minimal. The detector impedance is effectively that of the detector capacitance shunted by its leakage resistance, with the real part given by

$$\mathrm{Re}(Z) = \frac{R}{1 + \omega^2 R^2 C^2} \tag{4-13}$$

where

R = detector shunt resistance

C = detector capacitance, plus FET shunting capacitance.

The result of evaluating the integrals is

$$V_{nJ}^2 = \frac{kT}{C}\left[\frac{4}{RCF_R\pi^2}\ln\left(\frac{F_R\pi RC}{2}\right) + \frac{2}{\pi}\left(\frac{\pi}{2} - \tan^{-1}\frac{\pi RCF_R}{2}\right)\right] \quad (4\text{-}14)$$

For RC ~ 3 seconds, (i.e., $\epsilon = 3 \times 10^{-12}$ F cm^{-1}, $\rho = 10^{12}\,\Omega$cm):

$$V_{nJ}^2 = \frac{kT}{C}\left[\frac{4}{3\pi^2 F_R}\ln\left(\frac{3\pi F_R}{2}\right) + \frac{2}{\pi}\left(\frac{\pi}{2} - \tan^{-1}\left(\frac{3\pi F_R}{2}\right)\right)\right] \quad (4\text{-}15)$$

Relating this to a frame rate of 10 Hz yields $V_{nJ}^2 = 0.06\ kT/C$

The buffer FET noise is thermally induced noise in the drain current. To operate the BB as a linear shift register a high dc level, about which the signal may swing, must be introduced into the device. This causes the output to take the form of an amplitude-modulated square wave which in turn can be filtered by a rather narrow bandpass filter. The frequency at the output is N^2F_R. To preserve the integrity of the square wave (to ease sample and hold) the upper limit should be several times this frequency, or about 5 N^2F_R. The noise bandwidth for the output FET is then

$$\Delta f = 5N^2F_R - \frac{1}{2}N^2F_R = 4.5\,N^2F_R \quad (4\text{-}16)$$

The thermally induced drain noise current can be modeled by utilizing an effective noise resistor, R_n, at the gate of the FET. R_n is taken as $2/3(g_m)$ where g_m is device transconductance.[25] The gate referred noise voltage is given by

$$\bar{v}_{ng}^2 = 4kTR_n\Delta f = 4kT\left(\frac{2}{3g_m}\right)\left(4.5\,N^2F_R\right) \quad (4\text{-}17)$$

A lower limit on g_m is about $50 \times 10^{-6}\ (V_{gs} - V_T)$ so that

$$\bar{v}_{ng}^2 \approx \frac{2.5 \times 10^5}{(V_{gs} - V_T)}\,kTN^2F_R \quad (4\text{-}18)$$

where V_{gs} = gate-to-source voltage.

Assuming $V_{gs} - V_T = 1$, T = 300°K, and F_R = 10 Hz:

$$\bar{v}_{ng}^2 = N^2 \times 10^{-14}$$

The ratio of detector capacitance to total capacitance on the output gate is ~ 2/3. The amplifier noise referred to the detector is then

$$\bar{v}_{ngd}^{\,2} = \left(\frac{3}{2}\right)^2 \bar{v}_{ng}^{\,2} = 2.25 \times 10^{-14}\ N^2 \qquad (4\text{-}19)$$

The third noise component arises from the charge transfer process. During transfer, alternate FETs in the register are conducting as source follower amplifiers with capacitive loads.

If at $t = 0$, when transfer initiates, the voltage on the detector is at a level V_2 (the dc level being shifted through the register) then the detector voltage as a function of time during the transfer period is given by

$$v_d(t) = \frac{V_1 (V_1 - V_2)\, t/\tau + V_2}{1 + (V_1 - V_2)\, t/\tau} \qquad (4\text{-}20)$$

where

$V_1 = V_g - V_T$

V_g = clock voltage impressed on the FET gate

V_T = FET threshold voltage

$\tau = C/K'$

Adding a thermal noise component V_n to V_1 will add a noise component to $v_d(t)$. Detector Johnson noise introduces a second-order effect on the FET charging current which in turn alters the transfer noise. However, this source of noise will be small and is not considered. With the addition of the gate referred noise V_n, the detector voltage is

$$v_d(t) = \frac{(V_1 + V_n)^2\, t/\tau + V_2 \left(1 - [V_1 + V_n]\, t/\tau\right)}{1 + (V_1 + V_n - V_2)\, t/\tau} \qquad (4\text{-}21)$$

where

$$K' = \frac{\epsilon_{ox} \mu_p}{2 t_{ox}} \frac{Z}{L}$$

Z = FET channel width

L = FET channel length

μ_p = effective mobility of holes in the channel

t_{ox} = gate oxide thickness

ϵ_{ox} = permittivity of SiO_2

To a first-order approximation the noise contribution from Eq. (4-21) is

$$\bar{v}_{nt} = \frac{(V_1 - V_2)\ \bar{v}_n\ t/\tau}{1 + (V_1 - V_2)\ t/\tau} \tag{4-22}$$

The term $\bar{v}_n$ in Eq. (4-22) is given by

$$\bar{v}_n^{\,2} = 4kT\ R_n \Delta f \tag{4-23}$$

where

k = Boltzmann's constant (1.3804×10^{-23} joule/°K)

T = temperature in °K

$R_n = 2/3\ g_m$

The noise bandwidth Δf is set by the channel resistance and detector and FET shunting capacitance, with the channel resistance given by $1/g_m$. Thus

$$\Delta f = \frac{1}{2\pi C\ \ 1/g_m} = \frac{g_m}{2\pi C} \tag{4-24}$$

which leads to

$$\bar{v}_n^{\,2} = \frac{kT}{C}\left(\frac{4}{3\pi}\right) \tag{4-25}$$

The final noise on the detector due to the thermal noise introduced during transfer where the FET conducts for a time

$$T = \frac{1}{2 \times \text{clock frequency}} \text{ is:}$$

$$\bar{v}_{nt}(T) = \bar{v}_n \left[\frac{(V_1 - V_2)\, T/\tau}{1 + (V_1 - V_2)\, T/\tau} \right] \tag{4-26}$$

For the range of capacitor values and clock frequencies which would be encountered in a modest IC detector array, the term T/τ ranges from 5 to 1000. The term in brackets in Eq. (4-26) is thus approximately 1, and v_{nt} is then about equal to

$$\sqrt{\frac{kT}{C}\left(\frac{4}{3\pi}\right)}$$

This is the noise equal to one transfer. Since noise on a detector is indistinguishable from signal transfer noise it is additive and for n transfers

$$\bar{v}_{nt} = \sqrt{\frac{kT}{C}\,\frac{4}{3\pi}\,n}$$

The minimum number of transfers for a line of N detectors is 2N, i.e. two transfers per stage to attain directionality. Thus

$$\bar{v}_{nt}^{\,2} = \frac{kT}{C}\left(\frac{4}{3\pi}\right)2N \tag{4-27}$$

This analysis of transfer noise is not at all rigorous. The method employed integrates thermal noise contributions over the total time the FET conducts. Since the device is self-limiting (turning itself off after charge has been transferred), the pertinent noise contributions occur only during that portion of time when the FET is near cutoff. The value of v_{nt} is thus an overestimate of actual transfer noise.

The total noise referred to the detector is the sum of the three components

$$\bar{v}_N^{\,2} = \bar{v}_{nJ}^{\,2} + \bar{v}_{ngd}^{\,2} + \bar{v}_{nt}^{\,2} \tag{4-28}$$

$$= \frac{kT}{C}\left(0.06 + \frac{8N}{3\pi}\right) + 2.25 \times 10^{-14}\, N^2 \tag{4-29}$$

Thus, for frame rates of 10 to 30 Hz, the total noise of a bucket brigade pyroelectric array is

$$\bar{v}_N \approx \sqrt{\frac{8N}{3\pi}\,\frac{kT}{C}} \tag{4-30}$$

where it is assumed that the temperature fluctuation noise is negligible as is the case for X-Y addressed detector arrays (Section V).

The bucket brigade device is a dynamic device in that it depends on charge storage within the register for operation. During integration of the focused infrared scene, the registers are halted. Any defects in the silicon create localized high current regions. If the regions occur at charge storage sites within the circuit, nonuniform variations in the leakage currents from cell to cell will result. This nonuniform leakage, which corresponds to dark current variations in an optical sensor array, results in fixed pattern noise at the output. However, since the device is a storage device and capable of serial input, it can be utilized to cancel the FPN created within itself by frame storage and subtraction.

3. Cancellation of Fixed Pattern Noise

During one-half of a frame time the array is exposed to the scene and a latent image signal charge pattern is formed. Simultaneously, a fixed pattern of noise is formed over the array due to charge leakage. During the second half of the frame time, the scene is shuttered and as the detectors cool the inverse of the exposed signal pattern is formed but the same fixed noise pattern is generated. It is possible therefore to invert the signal from one-half frame, feed it back into the scanning register, and cancel the fixed pattern noise while at the same time doubling the signal level. Figure 4-7 illustrates the procedure.

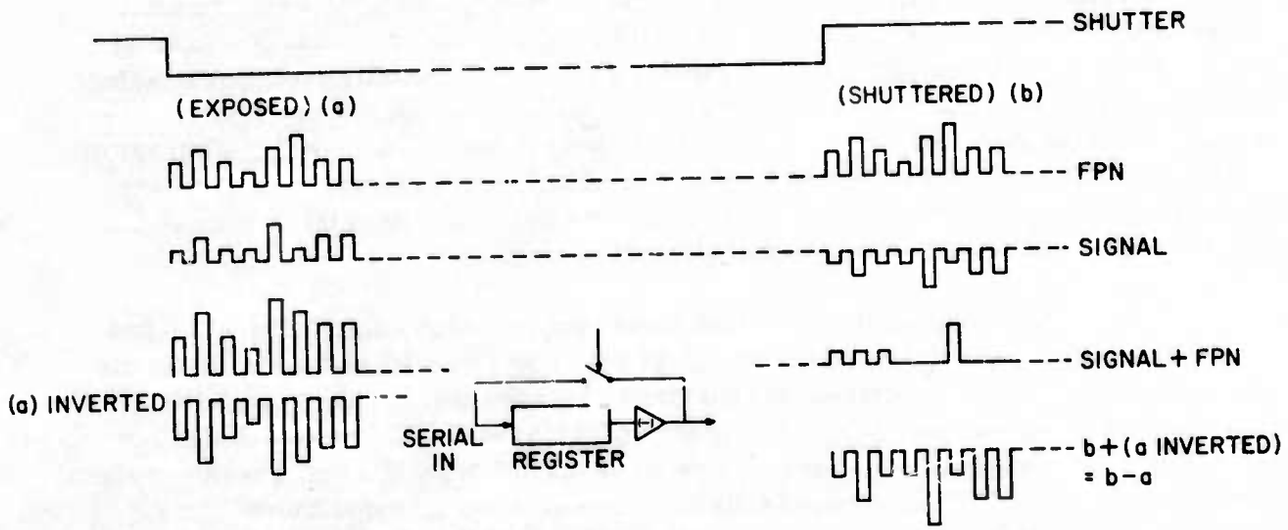


Fig. 4-7. Cancellation of fixed pattern noise in shuttered system of thermal detectors and bucket brigade scanner.

4. Poling

Poling the detectors of the BB circuit is easily accomplished. One detector electrode is accessible via the clock bus and the other is accessed via the register drain electrode by turning on all the register FETs. Alternatively, the second electrode may be accessed through the IC substrate. Thus it is possible to impose a poling potential directly across the detector. In addition, during operation of the array a potential is maintained across the detector, tending to prevent any spontaneous depoling that might occur.

5. Results

An amplifier feedback circuit was constructed (Fig. 4-8) to demonstrate FPN cancellation in a BB system. A 32-stage (64 transfers) integrated circuit register was utilized. The register was shielded from light so that the output signal was due only to dc bias and dark current variations. Operation of the device was made to conform to the operating mode of a TGS detector BB array. The feedback mechanism produced a reduction in FPN by a factor of 100. Figure 4-9 illustrates the BB output and the amplifier output. The signal illustrated is due to a serial dc input plus a localized dark current variation produced for an integration time of 0.05 seconds. Figure 4-10 shows the system outputs with and without feedback. In the test circuit, no attempt was made to cancel the sampling transients. Sample and hold was utilized in the feedback system to insure against the amplifier delay causing problems at the input.

A discrete component linear BB array containing 12 stages was constructed to test the pyroelectric bucket brigade circuit concept. The array was designed to allow the interchange of TGS detector capacitors with conventional capacitors having about the same capacitance. No degradation in operation as an analog delay line was noted when TGS capacitors were employed, as determined by comparison of signal to noise and the shapes of the resulting output waveforms. A pyroelectric signal was obtained from the array but responsivity was very low due to thermal sinking of the detectors and quantitative evaluation could not be made.

An integrated circuit linear TGS bucket brigade array containing 16 stages and corresponding to one line of the 16-by-16 array was then fabricated. The array was operated with undelineated detectors and without the thermal isolation slots. Figure 4-11 is a photomicrograph of portions of the array before application of the thin film TGS. Several arrays were operated as digital delay lines to determine signal transfer efficiency. The measured efficiency was 95% per transfer which (for the required 34 transfers) yields a net transfer efficiency of only 20%. The low transfer efficiency precluded any attempts to produce a thermal response from the detectors. It appears that the low transfer efficiency is associated with the fact that some of the FETs in the circuits were operating as depletion mode units. The inadvertent use of high resistivity silicon is believed to be responsible for this problem. Figure 4-12

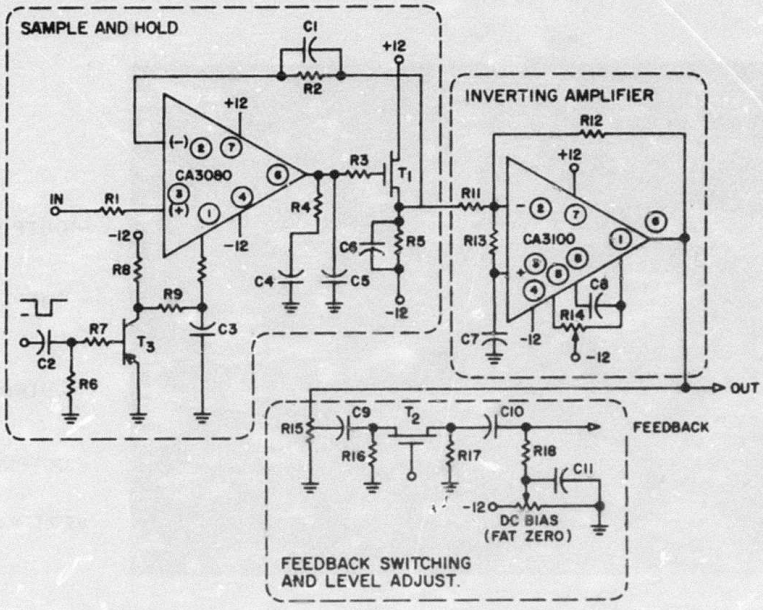


Fig. 4-8. Amplifier feedback circuit used for fixed pattern noise cancellation.

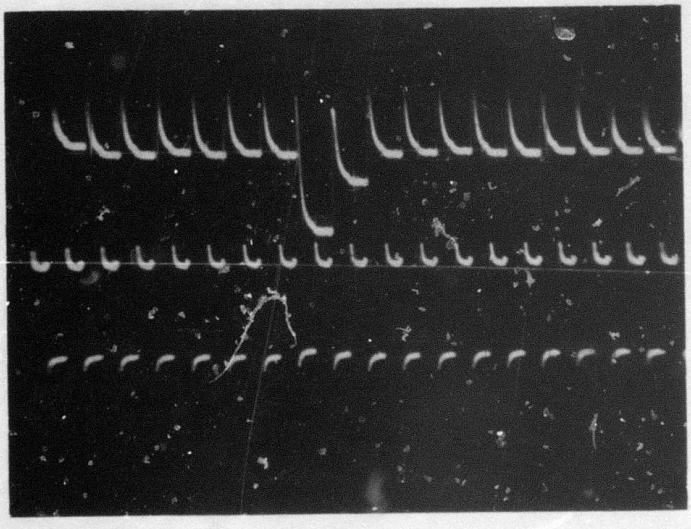


Fig. 4-9. Bucket brigade output and feedback circuitry output.

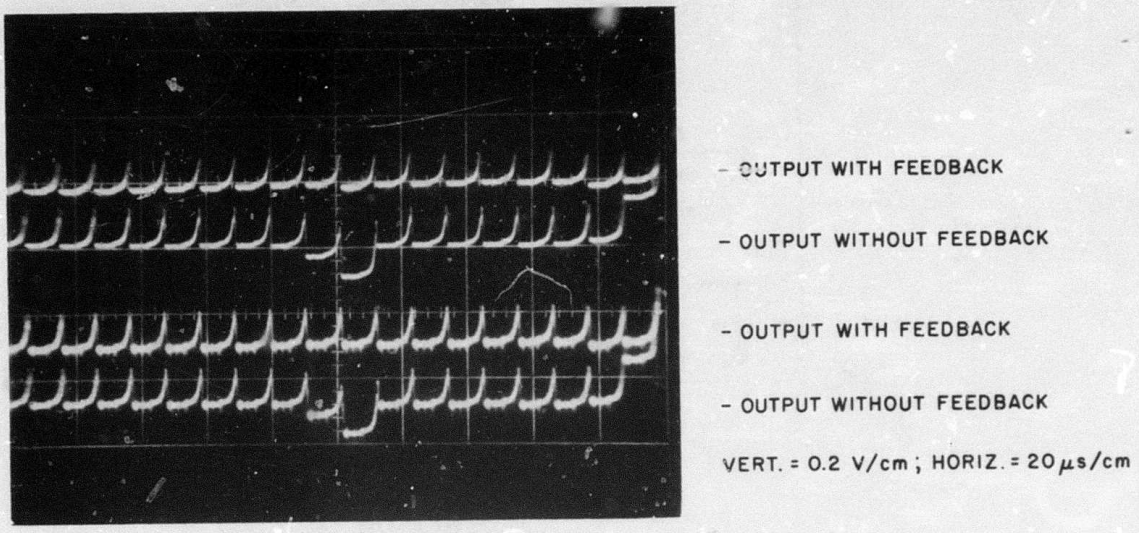


Fig. 4-10. Fixed pattern noise cancellation using feedback in a bucket brigade register.

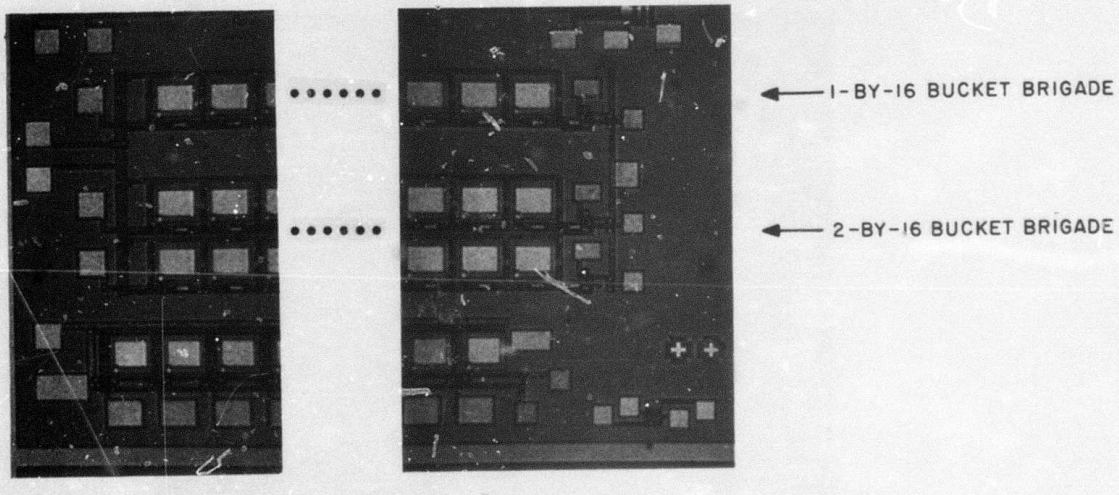


Fig. 4-11. Photomicrograph of a portion of the linear bucket brigade array prior to TGS deposition.

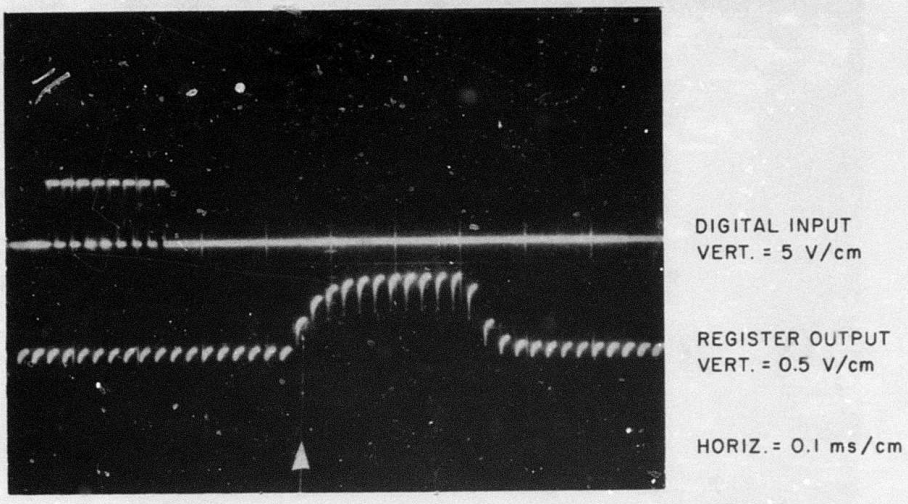


Fig. 4-12. Response of integrated BB register with TGS capacitors operated as a digital delay line.

shows the digital response of the array. The arrow on the photographs indicates where the first full digital "1" should appear at the output if the transfer efficiency were high. The output waveforms should have exactly the same number of pulses as the input. Poor transfer efficiency has caused the signal dispersion evident in Fig. 4-12. Signal dispersion can be particularly degrading to digital systems. For analog signals such as are extracted from the detector array, the effects of dispersion are not as degrading. The effects of poor transfer efficiency are to introduce a shading across the scene and loss of resolution from one edge of the scene to the other. However, high transfer efficiency is imperative if fixed pattern noise cancellation is to be employed.

One wafer of the 16-by-16 BB TGS array was completely fabricated including thermal isolation slots, but with undelineated detectors. The entire wafer was mounted on a ceramic substrate. One array was then wire bonded for electrical connection. The entire wafer was mounted intact so as not to risk breaking the SiO_2 detector-supporting membranes during chip dicing. This created a difficulty in wire bonding because of the large separation between the bonding pads of the array and the leads on the ceramic substrate. The completed assembly is shown in Fig. 4-13. The registers were successfully operated as delay lines. However, during operation in the integration mode it was not possible to insure that the output signal was being

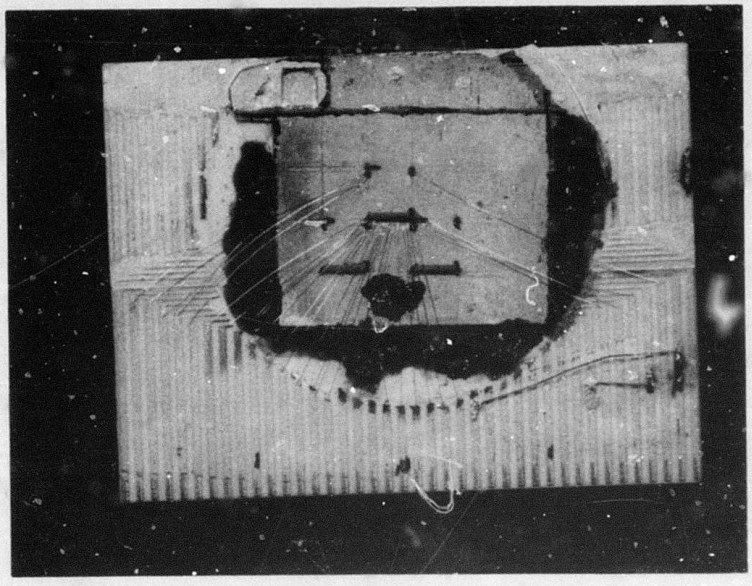


Fig. 4-13. Wafer of 16-by-16 TGS BB arrays with one array electrically connected.

derived from one detector. It was determined, however, that a definite pyroelectric response was derived and that simple dc poling of the detectors was effective.

Testing of the array registers to determine their transfer efficiency was performed. Initially the multiplexing register was clocked and a digital signal was applied to its serial input. Both the input and output signals are shown in Fig. 4-4. For a device having perfect signal charge transfer, the output should look exactly like the input. Rounding of the leading and trailing edges and the addition of pulses in the output signal is due to poor transfer efficiency. The transfer efficiency of this device is approximately 93% per stage. It appears that the low efficiency is due to the high resistivity of the silicon substrate. It is believed that this factor is causing punch-through (inadvertent channel conduction) to occur in the FETs during normal circuit operation.

Figure 4-15 shows the digital response of a typical BB register within the image sensor portion of the array. Transfer efficiency appears to be lower than that of the multiplexing register. Five possible reasons for the larger dispersion observed from the image sensor registers can be identified:

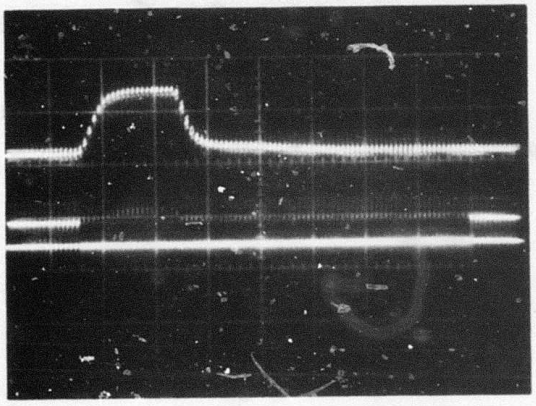
1. It is possible that punch-through of the clock-decoding FETs could be causing more than one scanning register to operate at the same time. Because of different signal delays from one register to the next, the output would have more pulses than the input, creating the appearance of lower transfer efficiency.

2. It is possible that coupling from the phase-two electrodes, located beneath the upper detector electrode, may be interfering with the clocking of phase-one, which is applied directly to the upper electrode.

3. It is possible that as a result of etching the thermal isolation slots the semiconductor properties in the vicinity of the FETs have been altered.

4. It is possible that the decoding transistors, through which the clocks are decoded to different registers, are adversely affecting the clock waveforms.

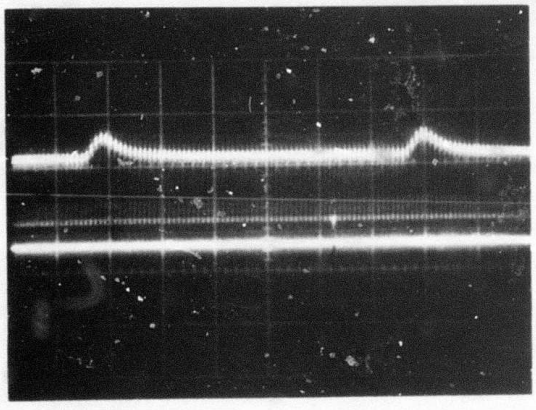
5. Finally, it is possible that because the TGS detectors were not delineated surface leakage may be affecting performance.



REGISTER OUTPUT
(VERT.= 2 V/cm)

REGISTER INPUT
(VERT. = 10 V/cm)

(HORIZ. = 0.2 μs/cm ; CLOCK RATE = 50 kHz)



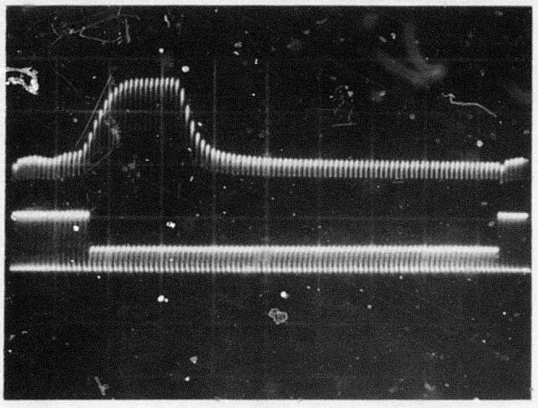
IMPULSE RESPONSE

REGISTER OUTPUT
(VERT. = 2 V/cm)

REGISTER OUTPUT
(VERT. = 10 V/cm)

(HORIZ. = 0.2 μs/cm ; CLOCK RATE = 50 kHz)

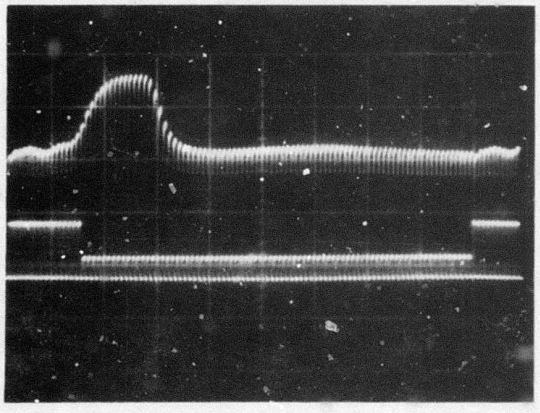
Fig. 4-14. Digital response of the multiplexing register.



REGISTER OUTPUT
(VERT. = 2 V/cm)

REGISTER INPUT
(VERT. = 10 V/cm)

(HORIZ. = 0.2 μs/cm; CLOCK RATE = 50 kHz)



REGISTER OUTPUT
(VERT. = 2 V/cm)

REGISTER INPUT
(VERT. = 10 V/cm)

(HORIZ. = 0.1 μs/cm; CLOCK RATE = 100 kHz)

Fig. 4-15. Digital response of typical scanning register with TGS capacitors.

An infrared source (a warm soldering iron) was placed in front of the array and chopped at about 30 Hz. The array was operated in the integration mode and a pyroelectric response was observed. However, quantitative measurements were not made because the signal may have been derived from more than one detector (two register clock inputs were not grounded and the registers may have been modulated by the upper electrode, resulting in an additive signal).

Since to date only one two-dimensional array has been partially tested and since that array was fabricated on very high resistivity starting material (20 ohm-cm) it is not possible to draw firm conclusions on the bucket brigade detector array concept.

Two-dimensional arrays are currently being fabricated on 3-5 ohm-cm starting silicon which should yield better transfer efficiency. Thorough evaluation of the two-dimensional bucket brigade detector concept will not be possible until these arrays are completed.

Section V

ANALYSIS OF PYROELECTRIC INTEGRATED CIRCUIT ARRAY PERFORMANCE

In this section an analytical assessment is made of the performance capabilities of X-Y and bucket brigade (BB) addressed infrared imaging systems containing two-dimensional arrays of thin film pyroelectric detector elements formed on integrated circuit substrates. The analysis assumes detector array configurations consisting of delineated and thermally isolated thin film triglycine sulfate (TGS) elements positioned on thin SiO_2 membranes which bridge slots etched into a silicon substrate. In this arrangement, loss of detector heat produced by the focused scene radiation is due primarily to sideways conduction along the SiO_2 detector supporting membrane and through the two detector electrode connecting strips that contact the silicon substrate material. Calculations are made of imaging system noise equivalent temperature difference (for targets viewed against a $300^{\circ}K$ background), of thermal loss and voltage responsivity of the detector elements, and of the various noise processes. These include detector Johnson noise, FET gate referred 1/f noise, temperature fluctuation noise, FET gate to drain noise, and bucket brigade charge transfer noise. Omitted from consideration are the effects of FET switching noise and the effects of any differences in the threshold voltages of the FETs contained within each sensor cell. The calculations cover a range of detector sizes and operating frame rates.

The results of the calculations show that uncooled X-Y addressed infrared imaging systems capable of a temperature resolution of nearly $0.4^{\circ}C$ should be possible at a frame rate of 10 Hz for arrays composed of 4-mil by 4-mil detectors on 8-mil centers. The use of larger detectors on correspondingly larger centers leads to further improvement in temperature resolution. For 10-mil by 10-mil detectors on 15-mil centers, for example, the calculations predict a noise equivalent temperature difference of $0.07^{\circ}C$.

The noise model developed for a pyroelectric bucket brigade sensor array (Section IV) predicts higher noise than for an X-Y addressed array. In part, the effects of increased noise are offset by the decreased FET shunting capacitance which results in somewhat greater voltage responsivity, but the net effect is degraded sensitivity as compared with an equivalent X-Y addressed system. For a bucket brigade imaging system operating at a frame rate of 10 Hz and composed by 4-mil by 4-mil detectors an $NE\Delta T$ of $2.0^{\circ}C$ is predicted, while for 10-mil by 10-mil detectors, $NE\Delta T$ is predicted to be $0.35^{\circ}C$.

A. ARRANGEMENT OF PYROELECTRIC/INTEGRATED CIRCUIT ARRAY

The arrangement of a pyroelectric detector on an integrated circuit array (either X-Y or BB addressed) is illustrated in Fig. 5-1. The pyroelectric elements are formed on top of a thin thermally grown SiO_2 layer which bridges slots etched into the integrated circuit substrate. In this manner, a high degree of thermal isolation is provided between the pyroelectric detectors and the unetched silicon regions which are in the form of long narrow beams. In the 16-by-16 TGS array designed in this program, the silicon beams are approximately 2 mils wide and 10 mils in height. The active area of each detector element is defined by the lower electrode, which

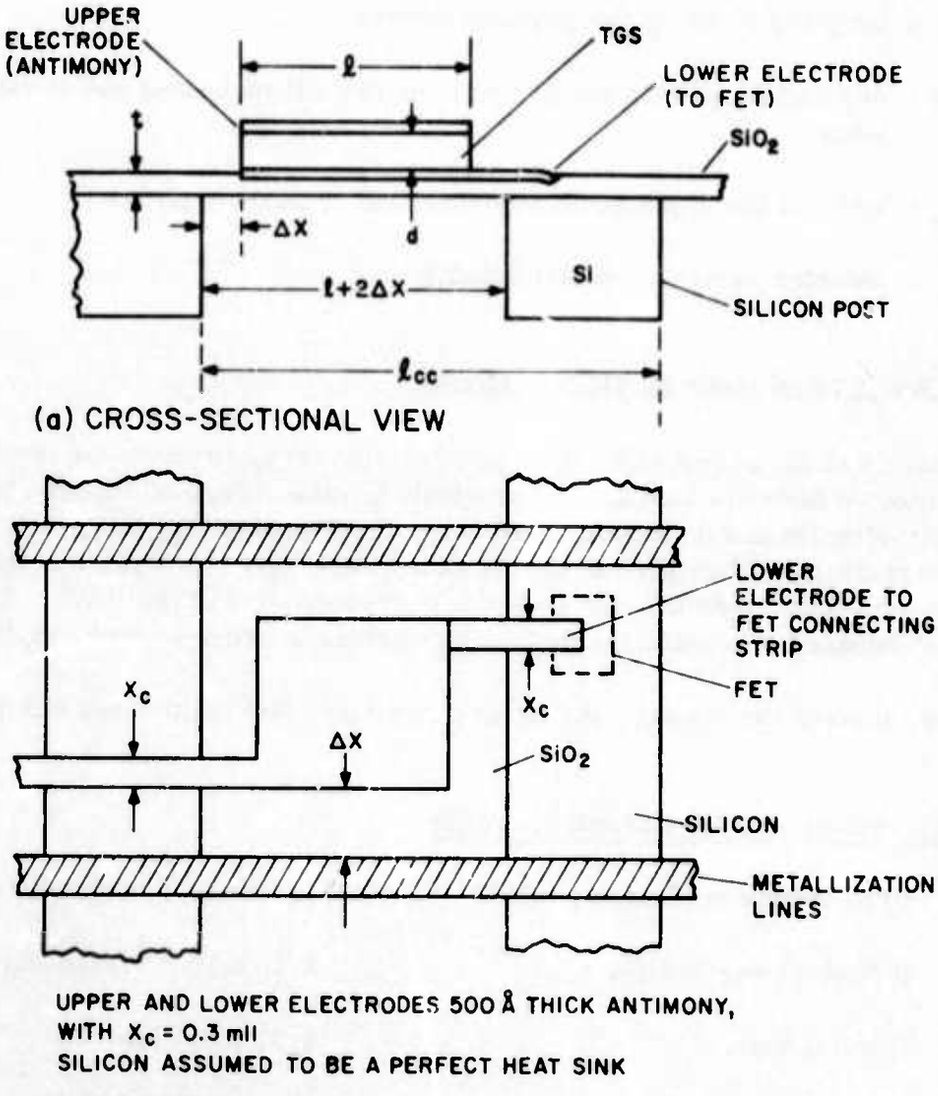


Fig. 5-1. Arrangement of a pyroelectric detector on a thermally isolated integrated circuit substrate.

is attached to an FET. The FETs, along with the diffused signal lines, are formed in the silicon substrate prior to etching of the slots. The unetched silicon beams prevent thermal crosstalk between detectors in the column direction (see Fig. 5-1). Similarly, the metallized lines which run over the surface of the SiO_2 membrane serve as thermal shunts between detectors located on a common row; accordingly these lines eliminate thermal crosstalk in the row direction. The dimensions given in Fig. 5-1 are defined as follows:

t = thickness of the SiO_2 supporting membrane

d = thickness of the pyroelectric material

ℓ = length of a side of the (square) detector

ΔX = separation between the detector and the silicon beams and metallization lines

X_c = width of the upper and lower electrode connecting strips

ℓ_{cc} = detector center-to-center spacing

B. PARAMETERS USED IN THE ANALYSIS

Analysis of the pyroelectric/integrated circuit array requires the consideration of a number of factors which are not precisely known. These include the magnitudes of the pyroelectric and dielectric coefficients of polycrystalline TGS, the thermal conductance of the thin films used in the detector electrodes, the dielectric loss tangent of the pyroelectric material, and the noise characteristics of the FETs. It has therefore been necessary to estimate certain parameters in order to perform the analysis.

The values of the detector and array properties used in this analysis are listed below:

Polycrystalline triglycine sulfate (TGS)

Pyroelectric coefficient, dP/dT	1.48×10^{-8} coulomb/cm^2 - ^oK*
Dielectric coefficient, ϵ	2.45×10^{-12} farad/cm*
Specific heat, C_p	0.97 joule/gm - ^oK
Mass density, ρ_m	1.69 gm/cm^3

*Averaged over the principal crystallographic directions

Other materials

Thermal conductivity (SiO_2), k_s[26]	1.18×10^{-2} W/cm - ^oK
Thermal conductivity (antimony electrodes), k_c[27]	0.2 W/cm - ^oK

C. THERMAL CONDUCTANCE AS A FUNCTION OF DETECTOR SIZE AND CENTER-TO-CENTER SPACING

The total thermal conductance for the detector arrangement illustrated in Fig. 5-1 is given by

$$G = G_C + G_R + G_K, \qquad (W/^\circ K) \qquad (5\text{-}1)$$

G_C is the thermal conductance associated with the transport of heat along the SiO_2 detector supporting membrane and through the two electrode connecting strips shown in Fig. 5-1, G_R is the radiative conductance, and G_K is the convective conductance. Assuming both sides of the detector radiate equally,

$$G_R = 8\eta_d \sigma T^3 A_d \qquad (5\text{-}2)$$

where

η_d = emissivity of the detector surface

T = temperature of the surroundings

A_d = detector area

σ = Stefan-Boltzmann constant (5.67×10^{-12} W/cm^2 - $^oK^4$)

G_K may be expressed as

$$G_K = hA_d$$

where the convection coefficient h is 2.81×10^{-4} W/cm^2 - ^oK for still air at a temperature of 300^{o}K and at a pressure of one atmosphere.

G_C, which is by far the largest of the three thermal conductance terms, is given by

$$G_C = \frac{k_s A_c}{\Delta X} + \frac{2k_c A_t}{\Delta X} \qquad (5\text{-}3)$$

where the previously undefined quantities are:

A_c = cross-sectional area for heat transport through the SiO_2 detector supporting membrane

A_t = cross-sectional area for heat transport through the electrode connecting strips

A_t is determined by the thickness of the antimony electrode films and the width of the connecting strips, taken to be fixed at 500 Å and 0.3 mils respectively. Thus in all of the calculations to be performed, A_t has a constant value of 3.81×10^{-9} cm^2. A_c however will vary with detector size, thickness of the SiO_2 membrane, and the spacing between the detector and the silicon sections and metallization lines. It is given to a very close approximation by

$$A_c = 4t \left[\ell + \left(\frac{\ell^2}{4} + \frac{\Delta X \, (\ell + \Delta X)}{2} \right)^{1/2} - \frac{\ell}{2} \right] (cm^2) \quad (5\text{-}4)$$

We wish to determine G_C for various detector sizes, i.e. various values of ℓ, as a function of ℓ_{cc}, the detector center-to-center spacing, for a representative frame rate of 10 frames/second and for a detector thickness of 10 μm and SiO_2 membrane thickness of 12,000 Å. It will be assumed that the silicon sections and the metallization lines to which the detector heat is conducted are heat sunk at 300°K. The results of the calculations for detectors ranging in size from 1 mil on a side to 10 mils on a side and for center-to-center spacings ranging from 3 to 17 mils are shown in Fig. 5-2. The large increase in G_C that occurs as ℓ_{cc} approaches the value ℓ + 2 mils is due to the decrease in ΔX which this condition reflects.

Values of G_R and G_K for the same conditions applicable to Fig. 5-2 (and assuming a detector emissivity η_d of 0.8) are listed in Table 5-1. Comparison of Fig. 5-2 with the values of G_R and G_K of Table 5-1 shows G_C to be between 2 and 4 orders of magnitude greater than either G_R or G_K.

D. DETECTIVITY AND NOISE EQUIVALENT TEMPERATURE DIFFERENCE

Figure 5-3 illustrates a generalized detector/FET preamplifier arrangement. Each detector element of the array is assumed to be a square ℓ units of length on a side and d units of length thick. P_{IRS} represents the infrared signal power incident upon the detector.

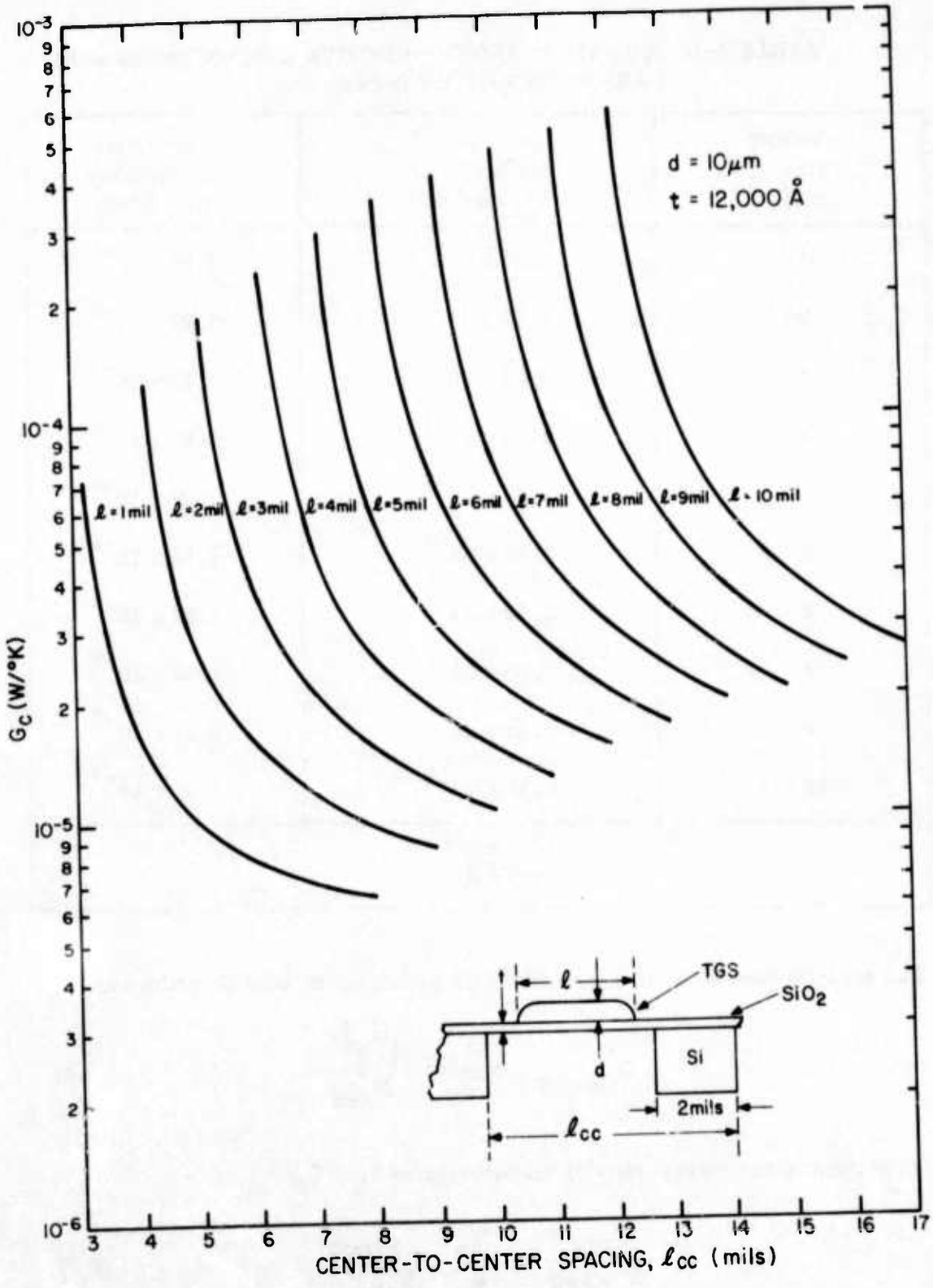


Fig. 5-2. Thermal conductance due to heat transport within SiO_2 membrane and detector connecting strips as a function of detector center-to-center spacing.

TABLE 5-1. RADIATIVE AND CONVECTIVE CONDUCTANCE FOR VARIOUS DETECTOR SIZES

Detector Size (mils)	Radiative Conductance G_R (W/°K)	Convective Conductance G_K (W/°K)
1	6.32×10^{-9}	1.81×10^{-9}
2	2.53×10^{-8}	7.24×10^{-9}
3	5.69×10^{-8}	1.63×10^{-8}
4	1.01×10^{-7}	2.90×10^{-8}
5	1.58×10^{-7}	4.53×10^{-8}
6	2.28×10^{-7}	6.52×10^{-8}
7	3.10×10^{-7}	8.32×10^{-8}
8	4.05×10^{-7}	1.16×10^{-7}
9	5.12×10^{-7}	1.47×10^{-7}
10	6.32×10^{-7}	1.81×10^{-7}
T = 300°K η = 0.8		

The specific detectivity of a detector/FET arrangement may be written as

$$D^*_{\Delta\lambda eff} = \frac{\bar{v}_s}{\bar{v}_N} \frac{\sqrt{A_d \Delta f}}{P_{IRS}} \qquad (5\text{-}5)$$

Since the voltage responsivity of the detector is $V_R = \bar{v}_s / P_{IRS}$,

$$D^*_{\Delta\lambda eff} = \frac{V_R}{\bar{v}_N} \sqrt{A_d \Delta f} \qquad (5\text{-}6)$$

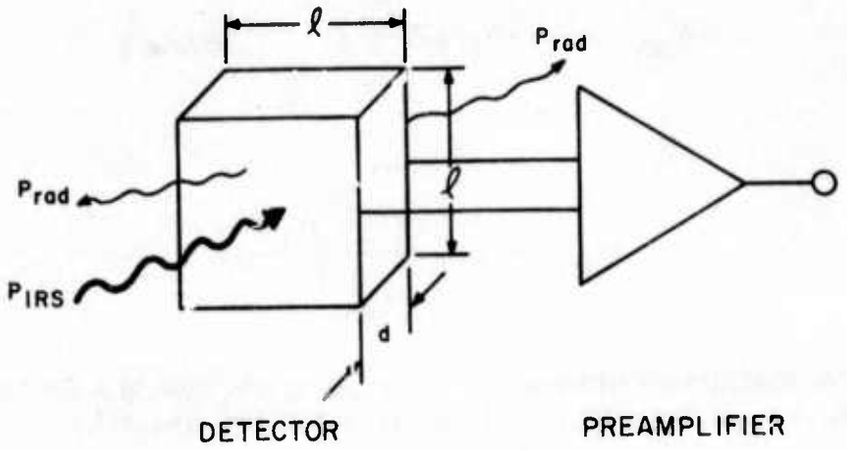


Fig. 5-3. A pyroelectric detector and its associated preamplifier.

which leads to

$$\frac{\bar{v}_s}{\bar{v}_N} = SNR = \frac{V_R}{\bar{v}_N} P_{IRS} \qquad (5\text{-}7)$$

In Eqs. (5-5) through (5-7),

v_s = rms signal voltage

$\bar{v}_N$ = total rms noise voltage, due to all sources, referred to the detector

A_d = detector area

Δf = detector noise bandwidth

SNR = signal to noise voltage ratio

$\Delta\lambda$ refers to the spectral interval of interest (8-μm to 14-μm)

For radiation over the 8- to 14-μm spectral interval,

$$P_{IRS} = (\Delta W_{\Delta\lambda})\, A_d \delta_{opt} / 4\, F_{NO}^2 \quad (W) \qquad (5\text{-}8)$$

where for a background temperature of T = 300°K,

$$\Delta W_{\Delta\lambda} = 0.38\,(4\eta\sigma T^3)\,\Delta T \qquad (W/cm^2) \tag{5-9}$$

which gives

$$P_{IRS} = \frac{0.38\,\eta\,\sigma\,T^3\,A_d\,\Delta T}{F_{NO}^{\,2}} \tag{5-10}$$

(The factor 0.38 arises because 38% of the power radiated by a 300°K blackbody is contained within the 8- to 14-μm spectral interval.)

In Eqs. (5-8) through (5-10),

$\Delta W_{\Delta\lambda}$ = radiant power, over the 8- to 14-μm spectral interval, per unit area incident upon the collector optics

δ_{opt} = optical transmission loss due to absorption and reflection by the collector optics

F_{NO} = system optical f/number

η = emissivity of the viewed object

σ = Stefan-Boltzmann constant (5.67×10^{-12} W/cm^2 - °K^4)

Substituting Eq. (5-10) into Eq. (5-7), and noting that when SNR = 1, $\Delta T = NE\Delta T$, the noise equivalent temperature difference, leads to

$$NE\Delta T = \frac{\bar{v}_N}{V_R}\,\frac{F_{NO}^{\,2}}{0.38\eta\sigma\,\delta_{opt}\,T^3 A_d} \qquad (°C) \tag{5-11}$$

Equation (5-11) shows that $NE\Delta T$ of a thermal imaging system is directly proportional to the total system noise voltage and decreases with increasing voltage responsivity. Both noise and voltage responsivity are affected by the mode of operation and accordingly bucket brigade and X-Y addressed arrays are expected to have different values of $\bar{v}_N$ and V_R. It is convenient to first consider the dependence of V_R upon the various material, device, and system parameters.

E. VOLTAGE RESPONSIVITY

The voltage responsivity of a pyroelectric detector is given by[1]

$$V_R = \frac{\eta_d \left[\omega \frac{dP}{dT} \quad \frac{RA_d}{G}\right]}{(1 + \omega^2 \tau_E^2)^{1/2} \quad (1 + \omega^2 \tau_T^2)^{1/2}} \quad (V/W) \qquad (5\text{-}12)$$

where

η_d = emissivity of the detector surface

ω = angular frame rate

τ_E = electrical time constant

τ_T = thermal time constant

G = total thermal conductance

R = parallel combination of the detector and preamplifier resistances

The above expression applies to detectors in either X-Y or bucket brigade addressed arrays.

1. Thermal Time Constants

The thermal conductance is, as noted earlier, independent of the mode of operation, as is the thermal time constant which is given by

$$\tau_T = \frac{H}{G} = \frac{H}{G_C + G_R + G_K} \quad \text{(seconds)} \qquad (5\text{-}13)$$

where H, the heat capacity of the detector is

$$H = m C_p = A_d d \rho_m C_p \quad (J/^\circ K)$$

and m is the mass of the pyroelectric detector material.

Plots of τ_T for the conditions previously referred to are shown in Fig. 5-4. As would be expected, τ_T increases with increasing detector size, and for any particular detector it increases with separation from the silicon section and metallization lines. It should be noted that for an "ideal detector", i.e., a detector for which G_C and G_K are zero and $G_R = 8\,\eta_d\,\sigma\,T^3\,A_d$, τ_T would be on the order of 1 second (assuming d = 10 μm, t = 12,000 Å and $\eta_d = 1.0$).

2. Electrical Time Constants

The only quantity in Eq. (5-12) that depends upon the mode of operation is the electrical time constant, τ_E. It differs because the FET capacitance shunting the detectors is larger in an X-Y addressed array than in a bucket brigade array.

Figure 5-5 shows the equivalent circuits for determining the electrical time constants of the two types of detector/FET arrangements being considered. In Fig. 5-5

C_d = detector capacitance

R_d = detector resistance

$\tan\delta$ = loss tangent of polycrystalline TGS

C_a = FET shunting capacitance

R_a = FET input resistance

R_{p-n} = series resistance of back-biased drain and source diffusions

C_G = FET gate-to-substrate capacitance

C_{g-s} = gate/source overlap capacitance

C_{g-d} = gate/drain overlap capacitance

In the X-Y addressed array, the FET input capacitance is the large gate-to-substrate capacitance, C_G, to which is added the much smaller gate/source and gate/drain overlap capacitances. However, in the bucket brigade arrangement the FET gate-to-substrate capacitance, C_G, does not shunt the detector directly but is in series combination with the resistance, R_{p-n}, of the back biased diodes formed by the drain and source diffusions of the FET. The RC time constant of this combination is so large that the gate-to-substrate capacitance is inconsequential to the circuit model. The capacitance, C_a, shunting the detector in the bucket brigade arrangement is thus the parallel combination of C_{g-d} and C_{g-s} and is much smaller than that of the XY structure.

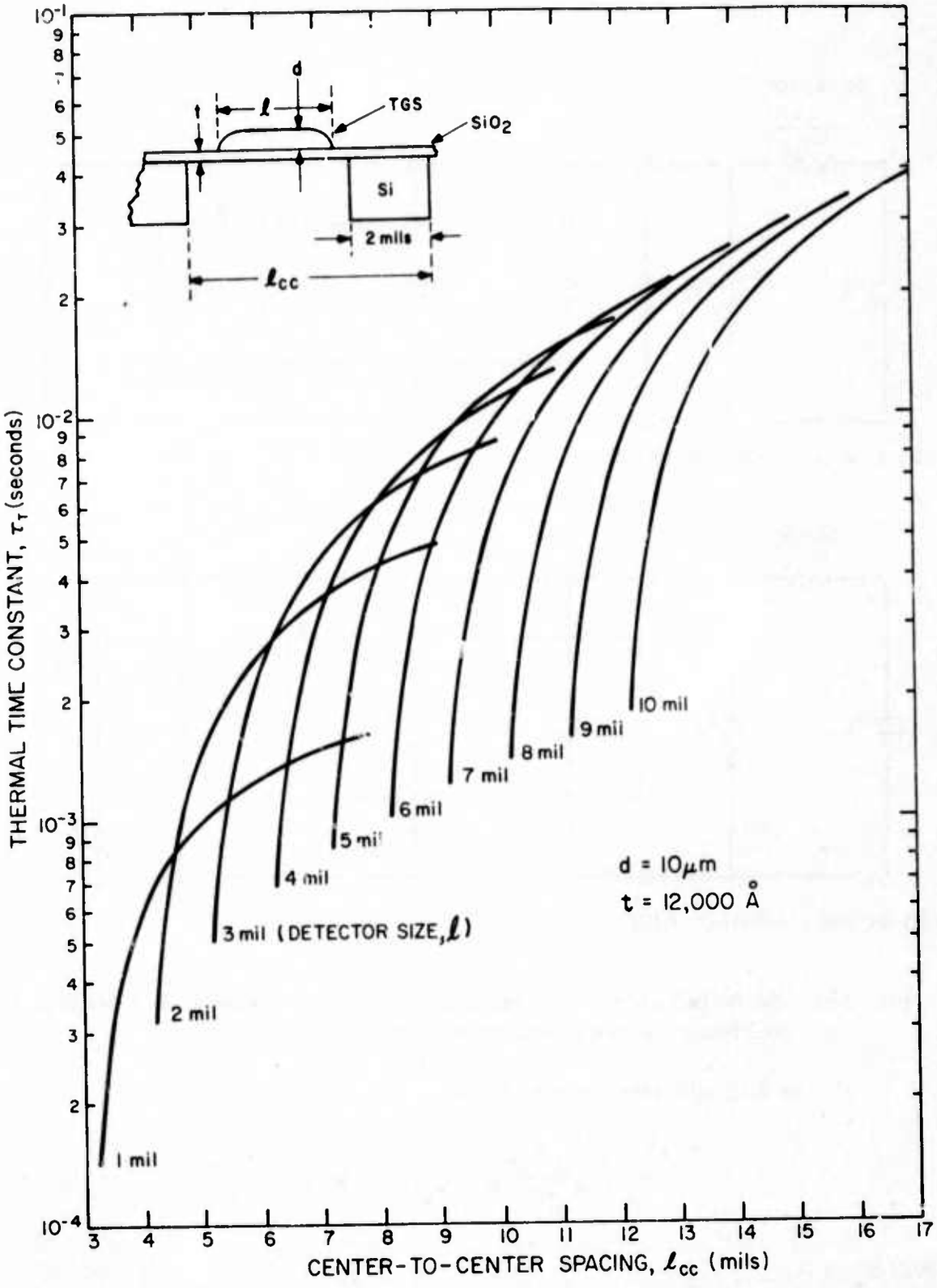
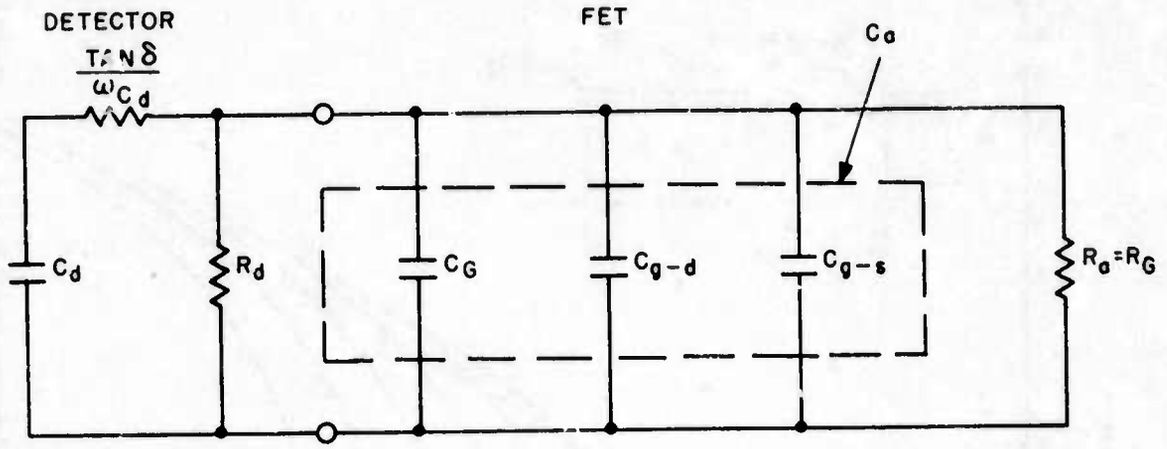
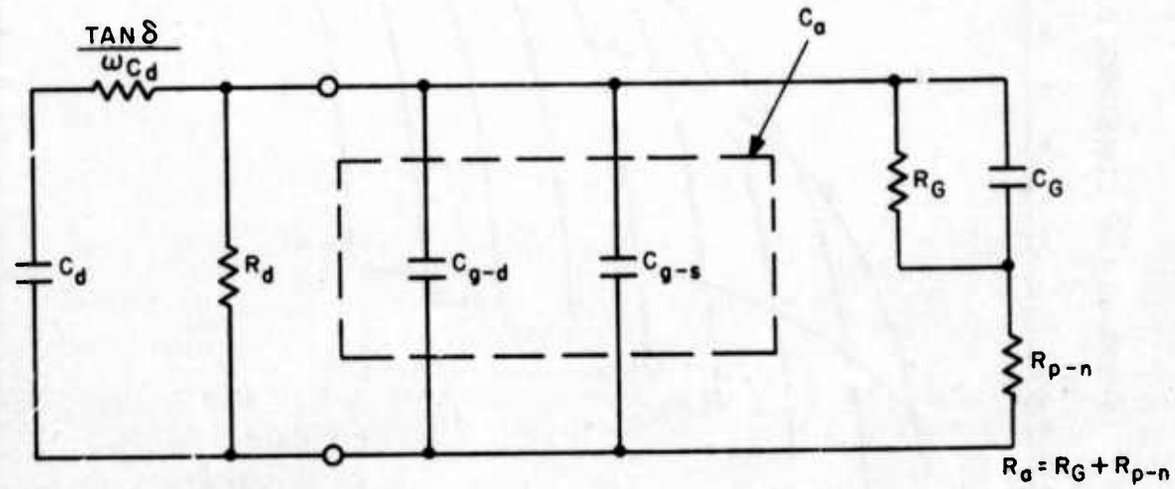


Fig. 5-4. Detector thermal time constant as a function of detector center-to-center spacing.



(A) X-Y ADDRESSED ARRAY



(B) BUCKET BRIGADE ARRAY

Fig. 5-5. Equivalent circuits for pyroelectric/FET elements in X-Y addressed and bucket brigade addressed arrays.

For an X-Y addressed array, τ_E is

$$\tau_E = \frac{R_d R_a}{R_d + R_a}(C_a + C_d), \qquad \text{(X-Y)} \qquad (5\text{-}14)$$

where $R_a = R_G$

and $C_a = C_G + C_{g-d} + C_{g-s}$

Since R_G (typically 10^{16} ohms) is much greater than R_d (which is between 10^{14} and 10^{12} ohms),

$$\tau_E \simeq R_d (C_a + C_d), \quad \text{(X-Y)} \tag{5-15}$$

Table 5-2 lists the calculated values of R_d, C_d, C_a and τ_E for detectors ranging in size from 1 mil by 1 mil to 10 mils by 10 mils. The values of R_d and C_d also apply to detectors of the same dimensions formed on a bucket brigade scanned array. For a bucket brigade addressed array,

$$\tau_E = \frac{(R_G + R_{p-n})\, R_d\, (C_d + C_{g-d} + C_{g-s})}{(R_G + R_{p-n}) + R_d} \quad \text{(BB)} \tag{5-16}$$

Since $R_G + R_{p-n} \gg R_d$,

$$\tau_E \simeq R_d (C_d + C_{g-d} + C_{g-s}), \quad \text{(BB)} \tag{5-17}$$

Values of τ_E for BB addressed arrays with detectors ranging in size from 1 mil by 1 mil to 10 mils by 10 mils on a side are shown in Table 5-3, for $C_{g-d} + C_{g-s} = 0.014$ pF, a typical value for aluminum gate PMOS FETs.

3. Variation of Voltage Responsivity with Detector Size

The variation in voltage responsivity with detector center-to-center spacing as calculated from Eq. (5-12) is shown for an X-Y addressed array in Fig. 5-6 (at a frame rate of 10 frames/second). It is seen that V_R generally decreases with increasing detector size; for any particular detector, it is seen to increase with separation from the silicon section and metallization lines.

The voltage responsivity of a bucket brigade addressed pyroelectric array will differ from that of an X-Y addressed array having the same size detectors only because the FET capacitance shunting the detectors is different in the two cases. As is evident from Eq. (5-12) one can write

$$V_{R_{(BB)}} / V_{R_{(X-Y)}} = (1 + \omega^2 \tau_E^2)^{\frac{1}{2}}_{(X-Y)} / (1 + \omega^2 \tau_E^2)^{\frac{1}{2}}_{(BB)} \tag{5-18}$$

and since $\omega^2 \tau_E^2 \gg 1$ in both types of arrays

$$V_{R_{(BB)}} / V_{R_{(X-Y)}} = (C_d + C_a) / (C_d + C_{g-d} + C_{g-s}), \tag{5-19}$$

TABLE 5-2. RESISTANCE AND CAPACITANCE OF 10-μm THICK TGS DETECTORS, ASSOCIATED FET PROPERTIES, AND ELECTRICAL TIME CONSTANTS FOR X-Y ADDRESSED ARRAYS

Detector Size, ℓ (mils)	Detector* Resistance R_d, (ohms)	Detector** Capacitance C_d, (pico F)	FET Area A_a, (mil^2)	FET*** Capacitance C_a, (pico F)	Electrical Time Constant τ_E, (seconds)
1	1.55×10^{14}	0.024	0.060	0.035	9.15
2	3.88×10^{13}	0.096	0.080	0.039	5.24
3	1.73×10^{13}	0.216	0.175	0.067	4.90
4	9.69×10^{12}	0.386	0.297	0.099	4.70
5	6.20×10^{12}	0.602	0.440	0.140	4.60
6	4.31×10^{12}	0.867	0.650	0.190	4.56
7	3.16×10^{12}	1.18	0.870	0.241	4.49
8	2.42×10^{12}	1.54	0.870	0.241	4.31
9	1.91×10^{12}	1.9[illegible]	0.870	0.241	4.18
10	1.55×10^{12}	2.41	0.870	0.241	4.11

*$\rho_d = 10^{12}$ ohm-cm (same for BB)
**Relative dielectric coeff. = 28.7 (same for BB)
***gate oxide thickness = 1,000 Å
FET Resistance = 10^{16} ohms (same for BB)

TABLE 5-3. ELECTRICAL TIME CONSTANT VERSUS DETECTOR SIZE FOR A BUCKET BRIGADE ADDRESSED TGS ARRAY

Detector Size, ℓ (mils)	Electrical Time Constant τ_E, (seconds)
1	5.89
2	4.27
3	3.98
4	3.88
5	3.82
6	3.80
7	3.77
8	3.76
9	3.76
10	3.76
Note: $C_{g-d} + C_{g-s} = 0.014$ pF	

The ratio of the voltage responsivity of a bucket brigade array to an X-Y addressed array for detectors of size ranging from 1 mil by 1 mil to 10 mils by 10 mils is shown in Fig. 5-7. It is seen that for detectors over the range $\ell = 2$ mils to $\ell = 7$ mils, the ratio is about 1.2. The higher ratio for detectors less than 2 mils in size arises because the FET gate capacitance in an X-Y array of very small detectors would be large compared to the detector capacitance (see Table 5-2). The ratio decreases, beginning for detectors 7 mils in size and extending to 10-mil detectors, because, as a practical matter, X-Y addressed arrays containing detectors in this size range could not be made with FETs any larger than those listed in Table 5-2. The selection of the FETs in Table 5-2 was governed by noise considerations for detectors over the range of $\ell = 2$ mils to $\ell = 7$ mils and by practical fabrication constraints for detectors outside this range.

E. DETECTOR/FET NOISE

The only quantity in the expression for NEΔT (Eq. (5-11)) remaining to be discussed is the imaging system noise voltage $\overline{v}_N$.

In an X-Y addressed array the total noise referred to the detector is

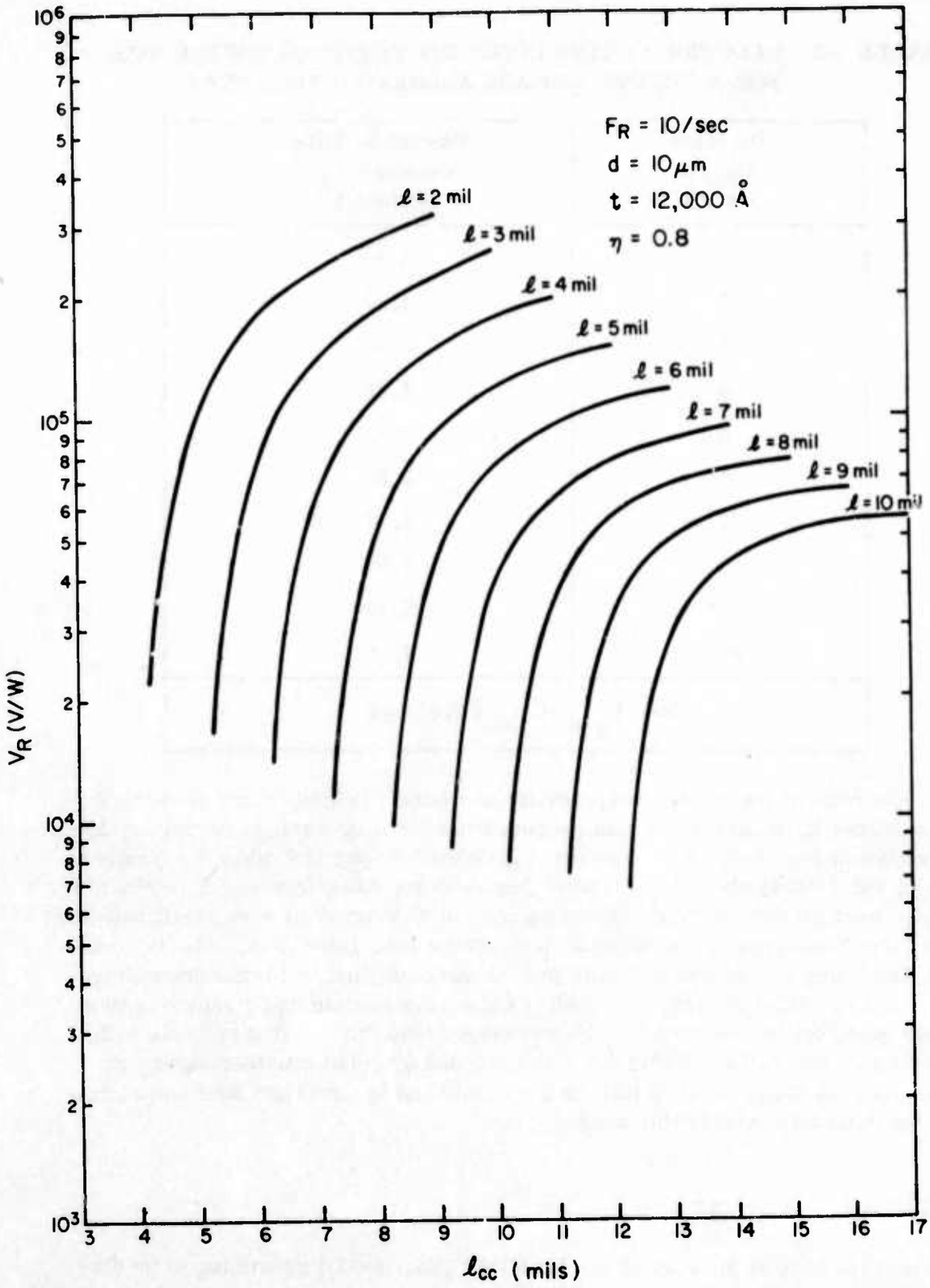


Fig. 5-6. Voltage responsivity as a function of center-to-center spacing (X-Y array).

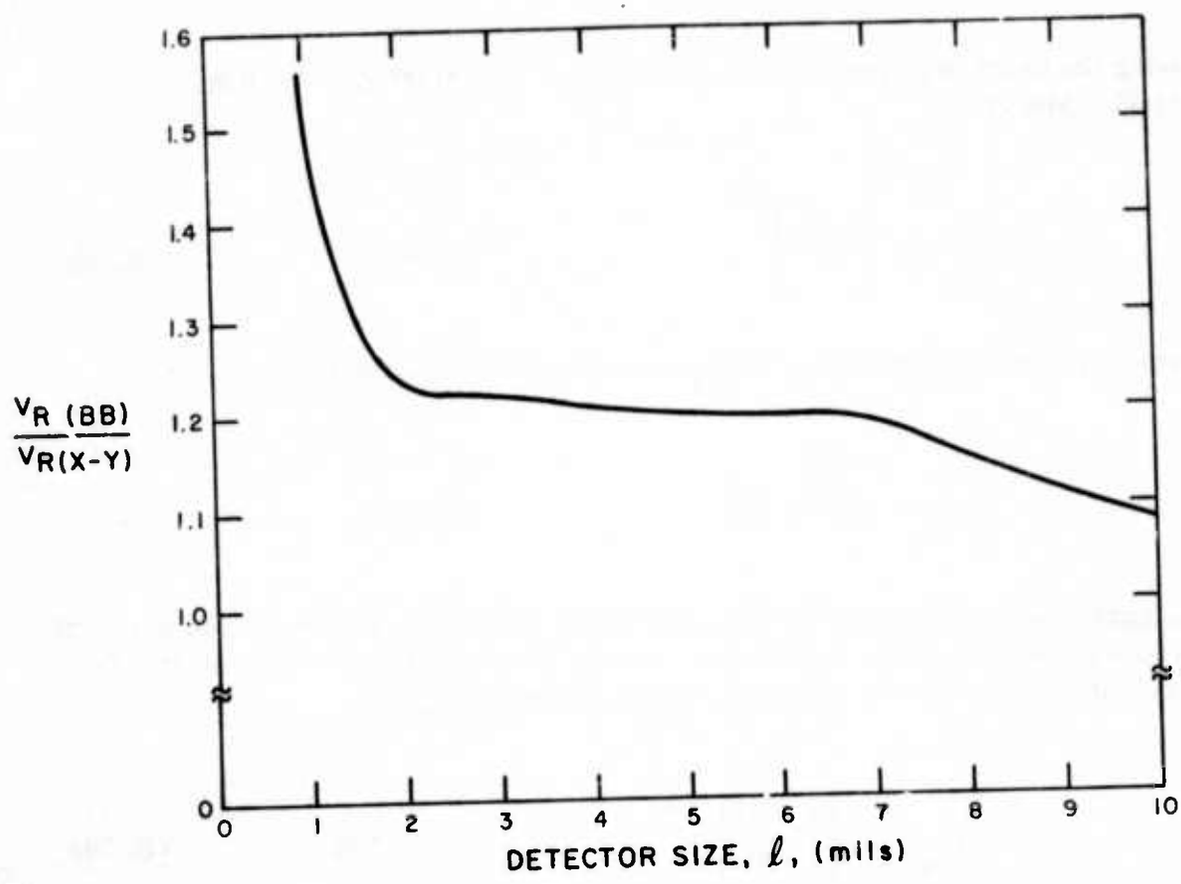


Fig. 5-7. Ratio of voltage responsivity of a bucket brigade to that of an X-Y addressed array, as a function of detector size ℓ.

$$\bar{v}_N = \left[\bar{v}_{nJ}^{\,2} + \bar{v}_{ng}^{\,2} + \bar{v}_{nT}^{\,2}\right]^{\frac{1}{2}} \tag{5-20}$$

where $\bar{v}_{nJ}$ is the Johnson noise, $\bar{v}_{ng}$ is the gate referred 1/f noise of the FET and $\bar{v}_{nT}$ is the temperature fluctuation noise.

The temperature fluctuation noise, which arises from either radiative exchange with the background or conductive exchange with the substrate, is the limiting noise process in all thermal detectors. A thermal detector in which the temperature noise is due solely to radiative exchange with the background is said to be at its theoretical limit. The rms temperature fluctuation $(\overline{\Delta T})$ is derived from:[28]

$$\Delta T^2 = \frac{2KT^2}{\pi G} \int_{\omega_\ell}^{\omega_u} \frac{d\omega}{1 + \tau_T \omega^2}$$

$$= \frac{2KT^2}{\pi G} \quad \frac{1}{\tau_T} \quad \tan^{-1} \quad \omega \tau_T \Big|_{\omega_\ell}^{\omega_u} \tag{5-21}$$

Taking the lower and upper angular frequency limits to be $\omega_\ell = 0$ and $\omega_u = \infty$, respectively, yields

$$\overline{\Delta T} = \left[\frac{KT^2}{H}\right]^{1/2} \quad (^\circ K \text{ rms}) \qquad (5\text{-}22)$$

The noise voltage associated with the temperature fluctuation is

$$\bar{v}_{nT} = \frac{V_R G}{\eta} \overline{\Delta T} \quad (V \text{ rms}) \qquad (5\text{-}23)$$

The gate referred 1/f noise of the input FET is dependent upon the length and width of the channel, the gate oxide capacitance, and the density of trapping states.[22] To a first approximation it is given (for a 32- by 32-element array) by

$$\bar{v}_{ng} = \left[\frac{4.16Q}{2\pi aL}\right]^{1/2} \quad (V \text{ rms}) \qquad (5\text{-}24)$$

where a is the channel width, L is the channel length and Q is a term that includes (among other parameters) the density of trapping states, the number of charge carriers flowing through the channel, and the oxide capacitance. For PMOS (p-channel metal-oxide-semiconductor) FETs of the type planned for use in the pyroelectric/integrated circuit arrays, Q is calculated to be 6.15×10^{-10} V^2 - mil^2.

The Johnson noise is given by

$$\bar{v}_{nJ}^2 = \frac{4KT}{2\pi} \int_{\omega_\ell}^{\omega_u} \text{Re}(Z)\, d\omega \qquad (5\text{-}25)$$

where K is Boltzmann's constant (1.38×10^{-23} J/°K) and Re (Z) is the real part of the detector/amplifier impedance. From the equivalent circuit of the detector/pre-amplifier combination, and assuming tan δ to be frequency independent,

$$\text{Re}(Z) = \frac{R\left[R\,\frac{\tan\delta}{\omega C} + \frac{\tan^2\delta}{\omega^2 C^2} + \frac{1}{\omega^2 C^2}\right]}{R^2 + 2R\,\frac{\tan\delta}{\omega C} + \frac{\tan^2\delta}{\omega^2 C^2} + \frac{1}{\omega^2 C^2}} \qquad (5\text{-}26)$$

For $\tan \delta^2 \ll 1$, and $\tan \ll \frac{1}{\omega \tau_E}$, Rc (Z) becomes

$$\mathrm{Re}(Z) = \frac{R}{1 + \omega^2 C^2 R^2} \tag{5-27}$$

Taking the lower limit to be $\omega_\ell = 0$, the upper limit to be $\omega_u = \infty$, and performing the integration leads to

$$\bar{v}^2_{nJ} = \frac{4\,KT}{2\,\pi\,C} \tan^{-1} \omega RC \Bigg|_0^\infty \tag{5-28}$$

which yields

$$\bar{v}_{nJ} = \left[\frac{KT}{C_d + C_a} \right]^{1/2} \tag{5-29}$$

The total noise $\bar{v}_N$, the Johnson noise, the temperature fluctuation noise voltage, and the gate referred 1/f noise are listed in Table 5-4 for TGS detectors ranging in size from 1 mil by 1 mil to 10 mils by 10 mils. The detectors are assumed to be 10-μm thick and the SiO_2 membrane is taken to be 12,000 Å thick. The values of the temperature fluctuation noise shown in Table 5-4 were calculated for ΔX = 1 mil for each detector, which represents a worst case (as will be evident later) since for minimum NE ΔT, ΔX will always be larger than 1 mil. For detectors up to 7 mils in size, the FET area was optimized to yield the minimum $\bar{v}_{ng}$. The FET area was not optimized for detectors larger than 7 mils because it becomes impractically large. The values of the detector resistance, detector capacitance, FET area, FET capacitance, and electrical time constant that apply to the calculated noise voltages of Table 5-4 are listed in Table 5-2.

F. NOISE IN BUCKET BRIGADE ARRAYS

The manner in which the total noise voltage can be estimated for a comparable bucket brigade array has been discussed in Section IV. By far, the largest source of noise is the transfer noise, $\bar{v}_{nt}$, and accordingly for a 32- by 32-element bucket brigade array one may write

$$\bar{v}_{N(BB)} \approx \bar{v}_{nt} = \left[\frac{27\,kT}{C_{g\text{-}d} + C_{g\text{-}s} + C_d} \right]^{\frac{1}{2}} \tag{5-30}$$

TABLE 5-4. NOISE VOLTAGE IN AN X-Y TGS DETECTOR ARRAY FOR VARIOUS DETECTOR SIZES

Detector Size (mils)	Total Noise Voltage v_n (microvolts)	Johnson Noise Voltage v_{nJ} (microvolts)	Temperature* Fluctuation Noise v_{nT} (microvolts)	Gate Referred 1/f Noise v_{ng} (microvolts)
1	298	286	19.3	82.3
2	214	201	19.2	71.3
3	149	141	14.0	48.2
4	115	109	11.1	37.0
5	93.5	88	9.13	30.4
6	78.4	73.9	7.72	25.0
7	67.7	63.9	6.73	21.6
8	61.7	57.5	6.23	21.6
9	56.8	52.2	5.76	21.6
10	52.6	47.7	5.34	21.6

For

$d = 10\,\mu m$
$t = 12,000$ Å
$\Delta X = 1$ mil
$F_R = 10$/second

*Maximum values of V_{nT}

Since Johnson noise is the largest source of noise in X-Y addressed arrays, it follows that

$$\frac{\bar{v}_{N(BB)}}{\bar{v}_{N(X-Y)}} = \left[\frac{(C_g + C_{g-d} + C_{g-s} + C_d)}{(C_{g-d} + C_{g-s} + C_d)}\right]^{\frac{1}{2}} \tag{5-31}$$

The ratio of the bucket brigade to X-Y addressed noise voltage is shown as a function of detector size in Table 5-5.

TABLE 5-5. RATIO OF $\bar{v}_{N(BB)}$ TO $\bar{v}_{N(X-Y)}$ FOR A 32- BY 32-ELEMENT ARRAY

Detector Size ℓ, (mils)	$\bar{v}_{N(BB)}/\bar{v}_{N(X-Y)}$
1	6.47
2	5.76
3	5.76
4	5.72
5	5.69
6	5.69
7	5.70
8	5.57
9	5.48
10	5.43

G. VARIATION OF NEΔT WITH DETECTOR SIZE AND CENTER-TO-CENTER SPACING

1. X-Y Addressed Arrays

The various terms contained in the expression for the NE ΔT of a pyroelectric/integrated circuit array have been discussed. It is now of interest to calculate NE ΔT as a function of detector center-to-center spacing for a number of detector sizes. Referring to Eq. (5-11), we will consider a thermal imaging system for which

$$F_{NO} = 1.0$$

$$\eta = 0.8$$

$$\delta_{opt} = 0.5$$

The system frame rate and the emissivity of the detector elements will be taken to be $F_R = 10$/second and $\eta_d = 0.8$, respectively, and the width of the silicon section is again taken to be 2.0 mils. The results of the calculations are shown in Fig. 5-8. The

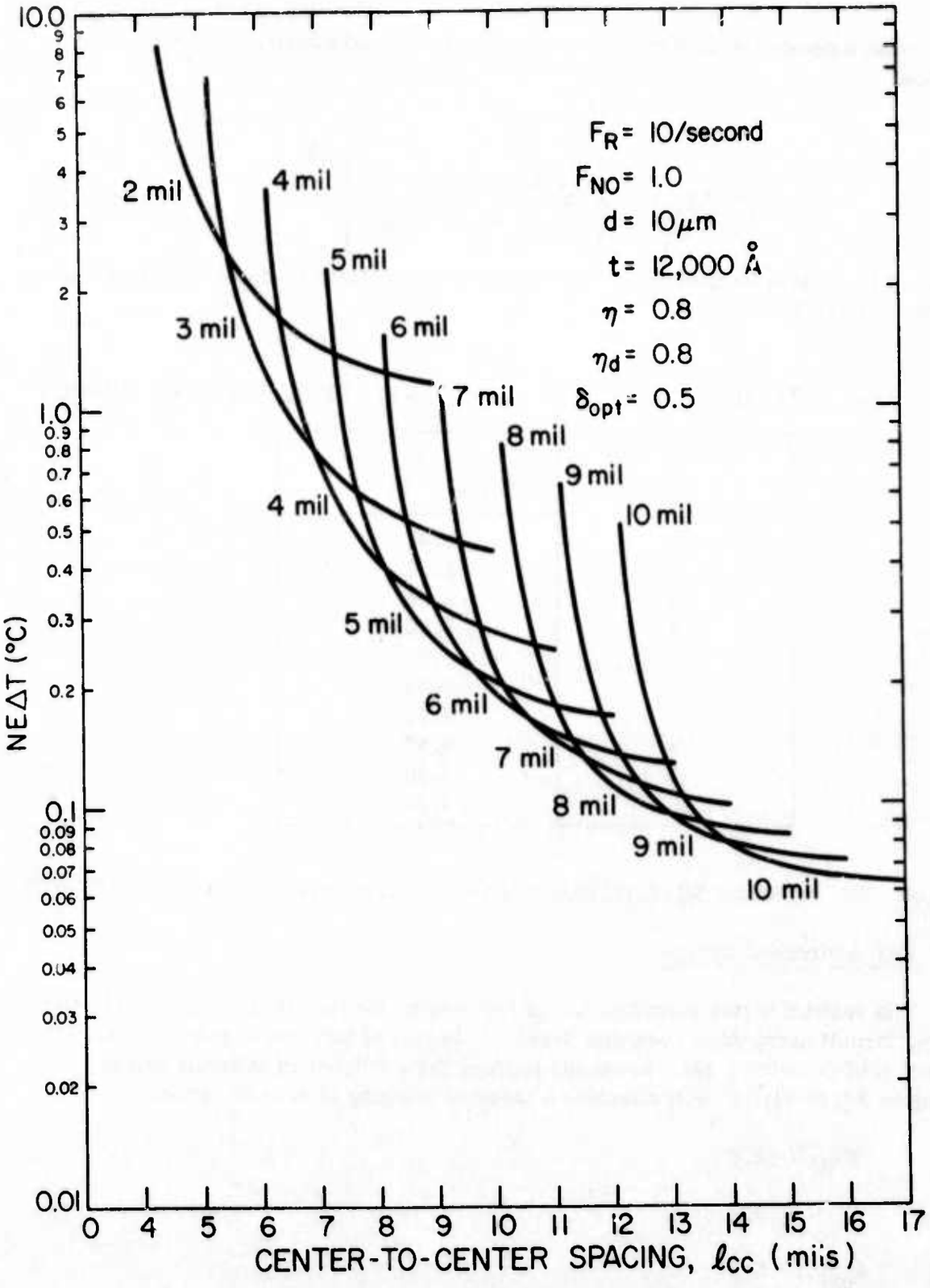


Fig. 5-8. Noise equivalent temperature difference as a function of center-to-center spacing (X-Y addressed array).

general character of the curves shows that, as expected because of decreased noise voltage, the temperature resolution improves with increasing detector size. The large increase in NE ΔT that occurs as the detector size approaches the value $\ell + 2\Delta X + 2$ mils is due to the accompanying large increase in G_C, which in turn results in reduced voltage responsivity. The relatively poor NE ΔT of the small 2- and 3-mil detectors is attributed to the larger Johnson noise associated with small detectors.

The detector size and center-to-center spacing of interest to the present program are $\ell = 4$ mils and $\ell_{cc} = 8$ mils. The data of Fig. 5-8 show that for a thermal imaging system composed of an array of such detectors, NE ΔT is predicted to be 0.42°C.

From Fig. 5-8, it is noted that the minimum NE ΔT for a particular center-to-center spacing is given by the lower bounding envelope of the family of curves. Figure 5-9 shows such curves for two frame rates, F_R = 10/second and F_R = 20/second, with the remaining parameters being identical to those of Fig. 5-8. The numbers along the two curves denote the optimum detector sizes (in mils) corresponding to the particular center-to-center spacings on which they are located. It is noted that for the detector geometry of interest in the developmental array (4-mil detectors on 8-mil centers), the increase in NEΔT that occurs in going to 20 frames/second is relatively small (0.42°C at 10 frames/second vs. 0.48 at 20 frames/second). It is also noted that there is virtually no change in NE ΔT for 2-mil detectors, which indicates that system degradation is appreciable even at 10 frames/second. In contrast, relatively low degradation in NEΔT occurs in the larger detectors. For example, for the 20-mil detector on 17-mil centers, NE ΔT at F_R = 10/second is 0.06°C, whereas at F_R = 20/second it increases to 0.12°C.

Figure 5-10, which is similar to Fig. 5-9, shows the variation in the minimum NE ΔT with center-to-center spacing at frame rates of 15/second and 30/second.

2. Bucket Brigade Addressed Arrays

Referring to Eq. (5-11), it is seen that the ratio of the NE ΔT of a bucket brigade addressed array to that of an otherwise identical X-Y addressed array may be written as

$$\frac{\text{NE } \Delta T \text{ (BB)}}{\text{NE } \Delta T \text{ (X-Y)}} = \left(\bar{v}_{N(BB)} / \bar{v}_{N(X-Y)}\right) \Big/ \left(\bar{v}_{R(X-Y)} / \bar{v}_{R(BB)}\right) \qquad (5\text{-}32)$$

which leads to

$$\frac{\text{NE } \Delta T(BB)}{\text{NE } \Delta T \text{ (X-Y)}} = \left[\frac{8N(C_d + C_{g\text{-}d} + C_{g\text{-}s})}{3\pi(C_d + C_G + C_{g\text{-}d} + C_{g\text{-}s})}\right]^{\frac{1}{2}} \qquad (5\text{-}33)$$

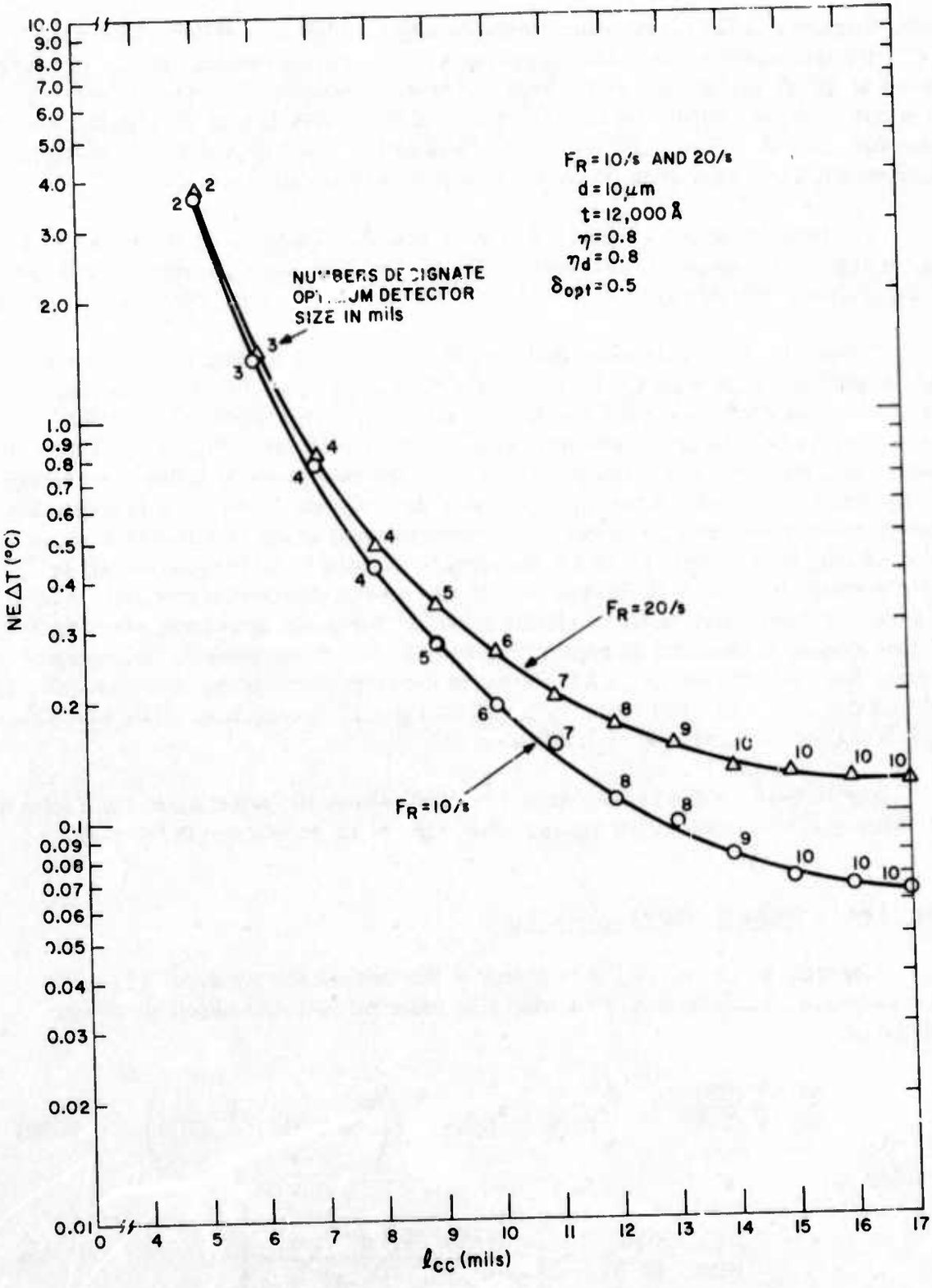


Fig. 5-9. Minimum NEΔT (noise equivalent temperature difference) as a function of center-to-center spacing (frame rates 10/second and 20/second; X-Y addressed array).

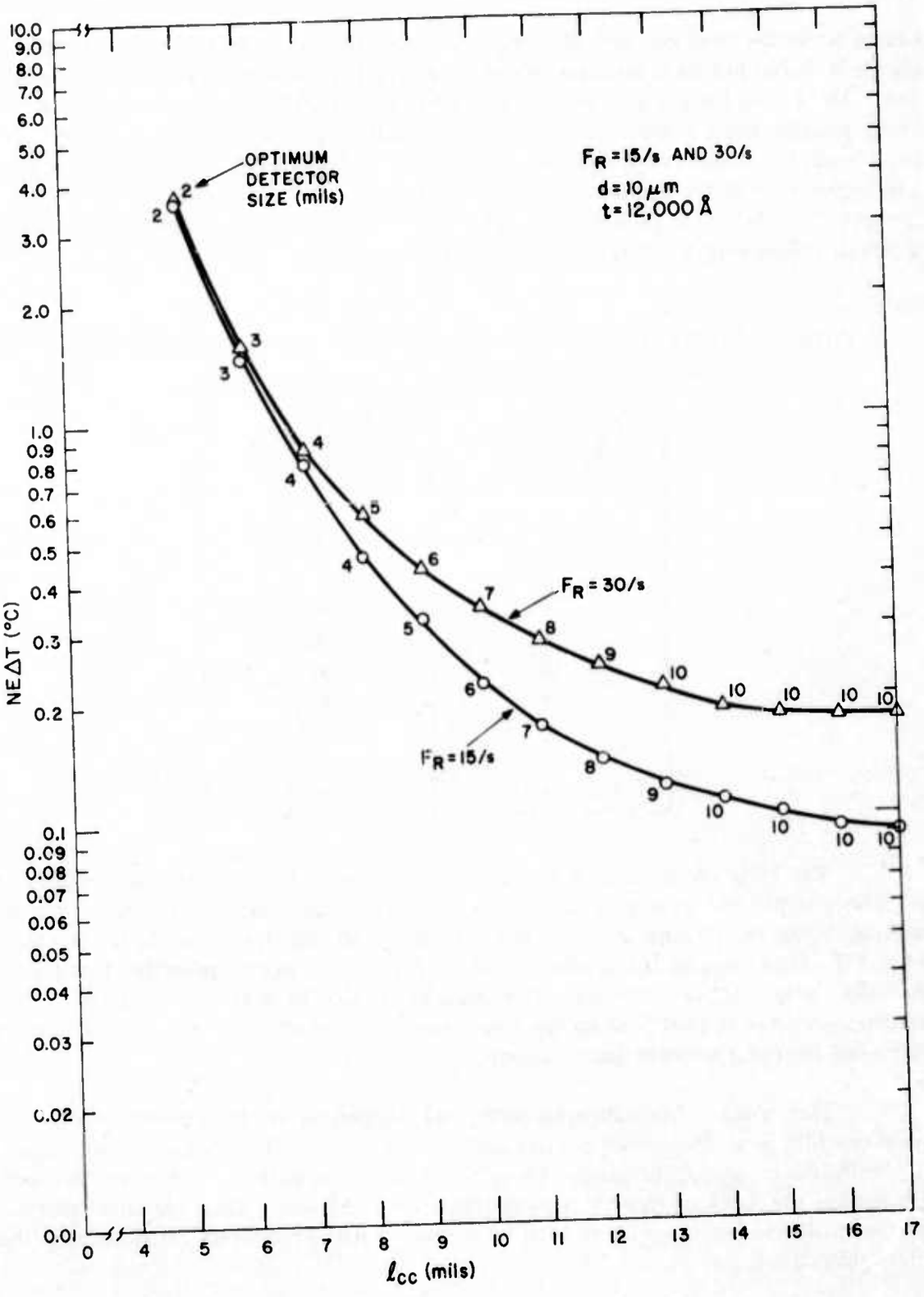


Fig. 5-10. Minimum NEΔT as a function of center-to-center spacing (frame rates 15/second and 30/second; X-Y addressed array).

where N^2 is the total number of elements contained within the array. The ratio is shown in Table 5-6 as a function of detector size for the conditions applicable to Fig. 5-8. As is seen from Table 5-6, a degradation in NEΔT relative to an X-Y addressed array ranging from a low value of 4.17 for 1-mil by 1-mil detectors to a high of 4.98 for 10-mil by 10-mil detectors is predicted. The degradation is attributed to the large noise predicted by the noise analysis of Section IV. It is believed that an actual pyroelectric bucket brigade array would not be as noisy as is predicted and that the noise in bucket brigade arrays has been overestimated.

TABLE 5-6. RATIO OF NEΔT (BB) TO NEΔT (X-Y) FOR THE CONDITIONS APPLICABLE TO FIG. 5-8

Detector Size ℓ, (mils)	$\frac{\text{NE}\,\Delta\text{T (BB)}}{\text{NE}\,\Delta\text{T (X-Y)}}$
1	4.17
2	4.68
3	4.68
4	4.72
5	4.74
6	4.74
7	4.79
8	4.84
9	4.94
10	4.98

The FETs in the bucket brigade array operate in a self-limiting mode, i.e., as charge is pumped onto a capacitor the FETs bias themselves off. Noise currents present during the charge transfer can only alter the charging rate, i.e., the current, but not the ultimate amount of charge transferred which is the quantity of interest. However, noise currents are effective when the device is near cut-off since 1) the superposed noise is rectified by the FET, and 2) its amplitude becomes larger than the quiescent charging current (near cut-off).

This tends to introduce an additional component of charge proportional to the size of the peak noise that occurs during this period. The present model does not ignore the noise during the active charging process and therefore does not properly account for the fact that the noise is rectified near cut-off. These factors tend to overestimate the noise. The amount by which the noise has been overestimated has not been ascertained.

H. VARIATION OF NE ΔT WITH SiO_2 MEMBRANE AND DETECTOR THICKNESS

The effect of increasing the SiO_2 membrane thickness is to increase the thermal conductance and accordingly to decrease the thermal time constant. The net effect is a reduction in voltage responsivity and in NE ΔT. This effect will be felt equally for either X-Y or bucket brigade addressed arrays. The manner in which NE ΔT varies with the thickness of the SiO_2 supporting membrane is shown in Fig. 5-11 for an X-Y addressed array composed of 4-mil by 4-mil detectors. At 8-mil center-to-center spacings the NE ΔTs for t = 10,000, 12,000, 18,000, and 24,000 Angstroms are 0.36, 0.42, 0.49 and 0.64°C respectively, showing that NE ΔT is a relatively sensitive function of the SiO_2 thickness. In a bucket brigade array the NE ΔTs corresponding to the same thicknesses of SiO_2 are estimated to be 1.7, 2.0, 2.3 and 3.0°C, respectively, based on the noise model of Section IV.

The dependence of NE ΔT of an X-Y addressed array composed of larger detectors upon SiO_2 membrane thickness is shown in Fig. 5-12 for 10-mil by 10-mil detectors the degradation in NE ΔT is seen to be relatively small at large values of ℓ_{ee}. For 10-mil detectors on 15-mil centers NE ΔTs for t = 10,000, 12,000, 18,000 and 24,000 Angstroms are 0.066, 0.069, 0.081 and 0.094°C, respectively. In an otherwise identical but bucket brigade addressed array the NE ΔTs for the same thicknesses are estimated to be 0.33, 0.34, 0.40, and 0.47°C, respectively.

The variation in NE ΔT with detector thickness is shown in Fig. 5-13 for an X-Y addressed array composed of 4-mil by 4-mil detectors at center-to-center spacings of 7, 8 and 9 mils. The NE ΔT values for comparable bucket brigade addressed arrays are estimated to be about 4.7 times greater than those shown in Fig. 5-13. It is seen that at a spacing of 9 mils, NE ΔT is relatively insensitive to detector thickness over the broad range of d = 12 μm to d = 20 μm. The improved temperature resolution attainable by increasing the center-to-center spacing to 11 mils is evident in Fig. 5-13. This improvement, of course, can only be obtained at the expense of an accompanying reduction in spatial resolution.

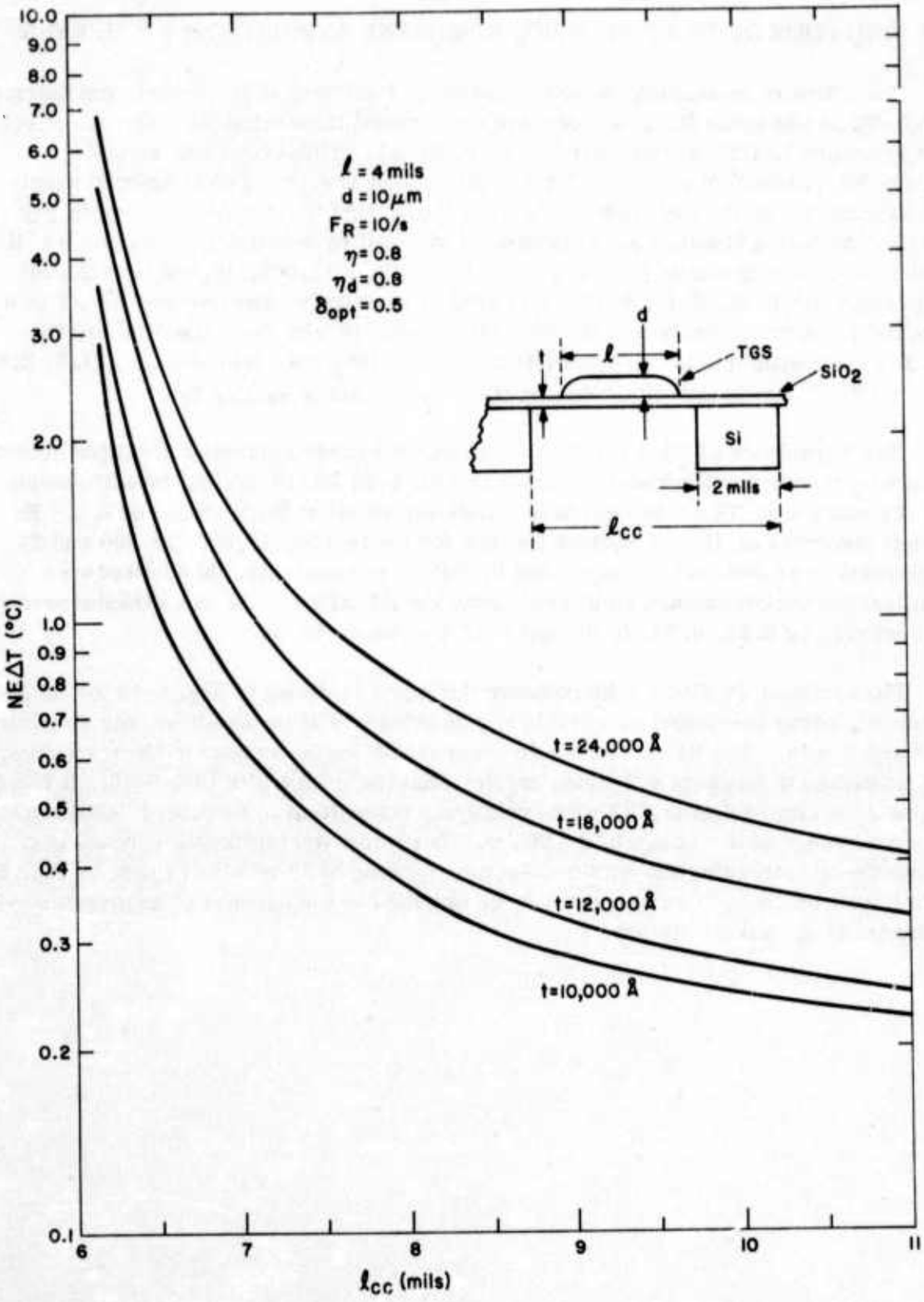


Fig. 5-11. NEΔT of 4-mil detectors as a function of center-to-center spacing for several SiO_2 membrane thickness.

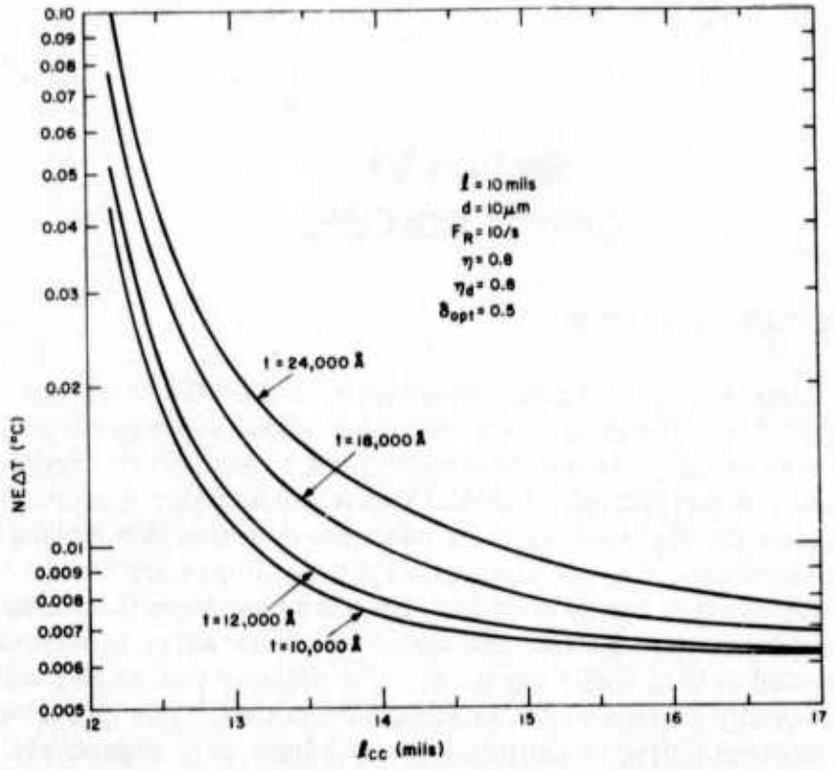


Fig. 5-12. NEΔT of 10-mil detectors as a function of center-to-center spacing for several SiO_2 membrane thicknesses.

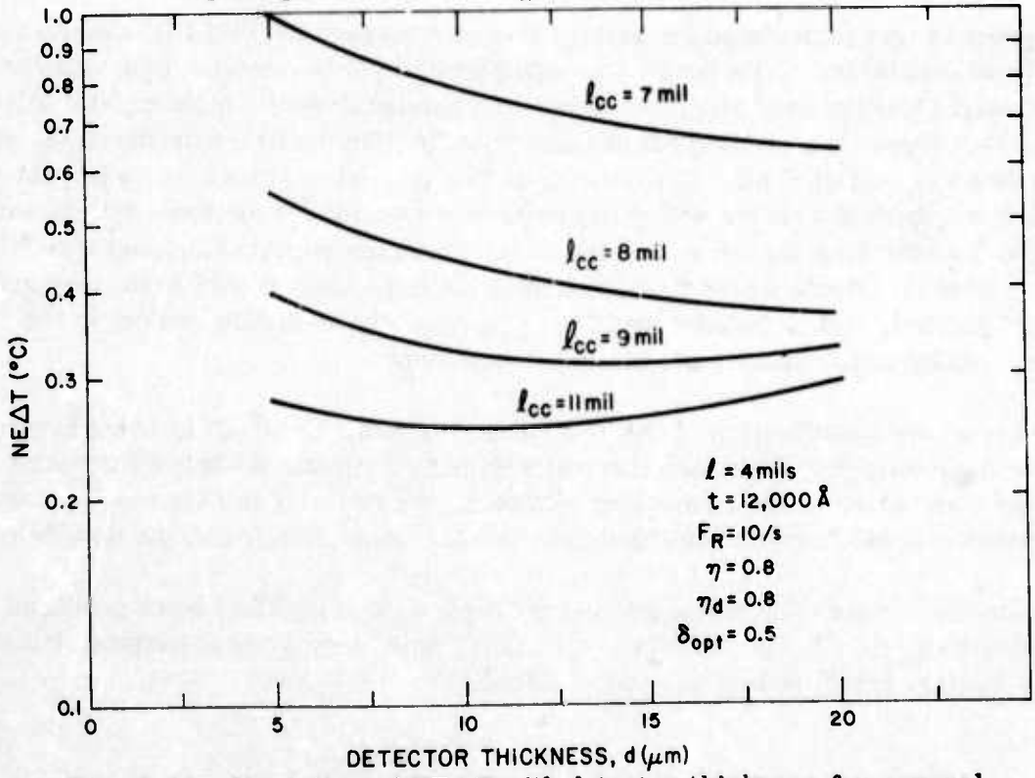


Fig. 5-13. Variation of NEΔT with detector thickness for several center-to-center spacings.

Section VI
CONCLUSIONS

A. ARRAY FABRICATION STATUS

A 16- by 16-element bucket brigade with polycrystalline TGS array was fabricated and shown to be operable. The detectors were easily poled, and a pyroelectric response was obtained from the array. Though the circuits tested showed poor transfer efficiency, the array concept was demonstrated. The fact that array register response was only slightly degraded from the multiplex register response indicates that etching the silicon slots can be done without harm to the adjacent circuitry. Improving transfer efficiency should pose no problem since bucket brigade delay lines have been fabricated with high efficiencies. Using frame storage and subtraction within the array to eliminate FPN has been demonstrated to be a viable approach. It is unlikely that an X-Y addressed array can be successfully fabricated due to poling difficulties. Though partial poling may be possible, uniform poling to saturation levels seems very improbable.

B. DEVELOPMENT OF THIN POLYCRYSTALLINE FILMS

A process was formulated for making thin polycrystalline TGS films in the range of 10- to 15-μm thick. Film purity was sufficiently high to produce detectors having voltage responsivities only slightly degraded as compared with single crystal TGS. The process relies upon the settling out of finely divided TGS particles produced by ball milling in a suspending fluid. Ball milling of TGS particles suspended in isopropyl alcohol in a polyethelyene jar with glass balls was found to be the most satisfactory technique for obtaining the submicrometer size particles required for uniform TGS films. The most effective way found to inhibit the solubility of TGS in the suspending isopropyl alcohol, and to thereby avoid the presence of the sulfate radical in the suspension, was by presaturating the alcohol with glycine.

Water vapor densification of the TGS films was found to result in films having higher voltage responsivities than thermally densified films. Although thermally densified films were found to have smoother surfaces, the reduced voltage responsivity and the inherent critical nature of thermal densification make this technique unsuitable.

Laser evaporated TGS films exhibiting the pyroelectric effect were produced using highly absorbing CO_2 laser radiation. The films have very smooth surfaces but degradation with time remains as a serious problem.

Broadening of the hysteresis loop of TGS by the addition of glycoic acid was accomplished. The broader hysteresis loop more nearly approaches the ideal square shape and may lead to improvement in its pyroelectric properties. However, since some conflicting evidence has been recently obtained, this matter requires further study before any firm conclusions can be drawn.

C. PYROELECTRIC/INTEGRATED CIRCUIT ARRAY TECHNOLOGY

No completely satisfactory approach to the problem of providing thermal isolation between thin film pyroelectric detectors and the integrated circuit substrate was developed. Primarily because of difficulties associated with providing thermal isolation, our goal of making and quantitatively evaluating the operation of small (16- by 16-element) image sensor arrays was not met. One 16- by 16-element bucket brigade array was completely fabricated late in the program and a pyroelectric response was observed. However, quantitative evaluation could not be made because it was not possible to ensure that the output signals were being derived from one detector.

The approach to providing thermal isolation by preferentially etching away the unwanted silicon would from time to time lead to clearly etched slots with the supporting SiO_2 membrane intact, but arrays having all of the slots clearly etched could not be reliably produced.

The best results were obtained using an ethylene diamine-catechol-water etch. At 90°C the etch rate in the (110) direction is about 1 mil per hour. Thermally grown SiO_2 can be used as an etch mask but the etchant slowly attacks the aluminum metallization and in the time required to etch through a wafer (8 to 10 hours) severe damage to the metallization occurs. No satisfactory masking material capable of reliably protecting the aluminum metallization was found, although a large number of materials were tested.

A special etching jig in which the face of the wafer containing the metallization is sealed from the etchant by means of an O-ring seal was used with some success. The chief problem with this arrangement was that the SiO_2 membranes were susceptible to cracking. The films, typically 12,000 to 20,000 Angstroms thick, were often found to be cracked immediately after etching. Subsequent handling often led to additional damage.

D. SINGLE CRYSTAL TGS ARRAY

Initial results using thin film microfingers were encouraging. Early in the program a complete assembly using a small wafer of 1-mil thick permanently poled TGS (grown from l-alanine solution) was made and tested. A peak-to-peak output of 30 mV was measured using an FET amplifier having an input capacitance of 4 pF. For the same conditions, a low capacitance amplifier should yield an output of 50 mV as compared with the theoretical value of 390 mV for an ideal detector.

The chief difficulty with this approach was in getting all of the chrome-gold microfinger contact springs to curl upward from the integrated substrate. Although the microfinger approach to producing a pyroelectric sensor array appears to be valid in principle, in practice a reliable procedure for fabricating large arrays of microfingers will first need to be developed. It appears that this will be a difficult task because of the large number of variables in the process that need to be optimized. A pair of metals other than chromium and gold might give a broader range of conditions for satisfactory deposition, but substantial further exploratory work would be required to demonstrate this.

E. DETECTOR ARRAY ARRANGEMENTS

The principle of the bucket brigade pyroelectric detector array appears to be sound, but additional development will be needed before a quantitative assessment can be made. In contrast to the X-Y addressed array, the detector elements can be easily poled and in actual operation the fields acting on the detectors tend to maintain them in a poled state. The bucket brigade approach also permits cancellation of fixed pattern noise by recycling the signal through the array and using its inherent frame storage and subtraction capabilities.

In common with X-Y addressed arrays, and for that matter in common with the pyroelectric vidicon, the achievable spatial and temperature resolutions are relatively low. It is believed that the noise model developed for the bucket brigade array overestimates the noise and that its temperature resolution capabilities would most likely be close to those of X-Y addressed arrays.

For either bucket brigade or X-Y addressed arrays, we believe that realizing detectors and center-to-center spacings smaller than the present 4-mil by 4-mil detectors on 8-mil centers will be extremely difficult. A major problem is posed by the silicon "real estate" required by the FETs and their address lines, the space required by thermal isolation gaps, and the detectors. The practical problem of aligning both sides of the wafer to obtain precisely aligned isolation slots is another limiting factor. Spatial resolution limitations on the same order also exist for pyroelectric vidicons. Here the spatial resolution is limited because of thermal spread along the vidicon's pyroelectric target. Whereas a detector element center-to-center spacing of 8 mils is achievable in a bucket brigade pyroelectric array, the effective element center-to-center spacing in a pyroelectric vidicon is significantly larger than 8 mils with single crystal targets and at frame rates of interest (10 to 30 Hz). However, it may be possible to achieve higher resolution if polycrystalline TGS targets are used because of reduced lateral thermal conductance and because the films can be defined by etching techniques.

F. RECOMMENDATIONS FOR FURTHER DEVELOPMENT

For moderately low temperature resolution (1 to 2°C) and moderately low spatial resolution (corresponding to 8-mil sensor spacings) applications, the bucket brigade pyroelectric sensor array appears to be a promising approach. A program to fully explore the potential of such arrays, initially in the form of linear arrays of 16 or so elements on 10-mil centers, should provide a quantitative assessment of the potential of such arrays, and a program of this type is recommended.

The polycrystalline thin film TGS techniques developed under this program could find application in other than image sensor arrays. Possibilities include quadrant detectors, arrays of quadrant detectors, and other types of target seeker arrays. A program to demonstrate the feasibility of such arrays, formed on thin mylar substrates and hybridized to integrated circuit preamplifiers, appears to have some merit. As presently envisaged, the pyroelectric elements along with the integrated circuits could be mounted on a common ceramic circuit board to provide a compact, low-cost target seeker assembly.

The use of polycrystalline TGS films as vidicon targets should be explored to determine if higher spatial and temperature resolution will result. The films can be prepared as large area samples and it may be possible to fill them with a material that will reduce their electrical resistance. Possible deleterious effects resulting from beam landing characteristics on the irregular thin film TGS surfaces will need to be explored.

Finally, the preferential etching techniques developed under this program could prove to be valuable in forming large scale line scan visible sensor arrays, the problem being that of butting a number of smaller arrays together to form a much larger array. It appears that the etching techniques developed permit one to etch close to the active regions of FETs without altering their properties. Accordingly, it is recommended that the etch process be further explored as a possible means for abutting visible sensor arrays with minimum loss of sensor elements.

REFERENCES

1. E.H. Putley, "The Pyroelectric Detector", in Semiconductors and Semimetals, Vol. 5, R.K. Willardson and A.C. Beer, Eds., Academic Press, New York: 1970, Chapter 6.

2. S. Hoshino, T. Mitsui, F. Jona and R. Pepinsky, "Dielectric and Thermal Study of Tri-Glycine Sulfate and Tri-Glycine Fluoberyllate", Phys. Rev., Vol. 107, no. 5 (Sept. 1, 1957), pp. 1255-1258.

3. H. Beerman, "Pyroelectric Infrared Radiation Detector", Ceramic Bulletin, Vol. 46 (1967), pp. 737-740.

4. R.F.G. Taylor and K.E. Trezise, "Pyroelectric Materials for Thermal Imaging", SERL Technical Journal, June 1971, pp. 5.1-5.14.

5. P.J. Lock, "Doped Triglycine Sulfate for Pyroelectric Applications", Applied Physics Letters, Vol. 19, no. 10 (1971), p. 390.

6. F. Jona and G. Shirane, Ferroelectric Crystals, MacMillan, New York: 1962, Chapter II: "Tri-Glycine Sulfate and Isomorphous Crystals".

7. M.R. Holter et al., Fundamentals of Infrared Technology, MacMillan & Co., New York: 1962, pp. 146-149.

8. A. Stoller, "The Etching of Deep Vertical-Walled Patterns in Silicon", RCA Review, Vol. 31, no. 2 (June 1970), pp. 271-275.

9. J. Chapelle and L. Taurel, "Proprietes Dielectrique d'un monocristal de sulfate de glycocolle particllement deutere", Compt. Rend., Vol. 249 (1959), pp. 1332-1333.

10. S.R. Fletcher, A.C. Skapski and E.T. Keve, "Crystallographic Studies of Irradiation/Field Treated Triglycine Sulfate: a New Structure Form", Jour. Phys. C: Solid State Physics, Vol. 4, no. 11 (Aug. 14, 1971), pp. L255-L258.

11. B. Brezina, "Growth and Characterization of Solid Solutions of Ferroelectric TGS Single Crystals with Isomorphic Compounds", Materials Research Bulletin, Vol. 6 (1971), pp. 401-412.

12. E.T. Keve, K.L. Bye, P.W. Whipps and A.D. Annis, "Structural Inhibition of Ferroelectric Switching in Triglycine Sulfate - I: Additives", Ferroelectrics, Vol. 3 (1971), pp. 39-48.

13. S. Triebwasser, "Study of the Second-Order Ferroclectric Transition in Tri-Glycine Sulfate", IBM Journal of Research and Devclopment, Vol. 2, no. 2 (July 1958), p. 212.

14. B.T. Matthias, C.E. Miller and J.P. Remeika, "Ferroelectricity of Glycine Sulfate", Physical Review, Vol. 104, no. 3 (Nov. 1, 1956), p. 849.

15. J.B. Price and I. Estricher, "Chemical Physics of the KOH-H_2O-Isopropyl Alcohol Silicon Etch System", Extended Abstracts of the Spring Meeting -- Electrochemical Socicty, Washington, D.C.: May 9-13, 1971, pp. 150-151.

16. D.B. Lee, "Anisotropic Etching of Silicon", Jour. Appl. Phys., Vol. 40, no. 11 (Oct. 1969), pp. 4569-4574.

17. R.M. Finne and D.L. Klein, "A Water-Amine-Complexing Agent System for Etching Silicon", Jour. Electrochemical Society, Vol. 114 (1967), pp. 965-970.

18. A Boornard, et al., "Pyroelectric/Integrated Circuit Infrared Imaging Array Development", Air Force Technical Report AFAL-TR-72-406 (Interim Technical Report on Contract F33615-72-C-1804).

19. M.J. Rand and J.F. Roberts, "Silicon Oxynitride Films from the NO-NH_3-SiH_4 Reaction", Extended Abstracts of the Spring Meeting -- Electrochemical Society, Washington, D.C.: May 9-13, 1971, pp. 216-217.

20. BDH Chemicals, Ltd., Poole, England BH124NN, Catalog of "Optran Crystal Growing Materials", October 1969, p. 8 (US representative: Gallard-Schlesinger Chemical Mfg. Corp., 584 Mineola Ave., Carle Place, Long Island, New York 11514).

21. S. Weiner, "Pyroelectric Infrared Radiation Detectors", presented at the Electro-Optical Systems Design Conference, New York: September 16-18, 1969.

22. S. Christensson, I. Lundstrom and C. Svensson, "Low Frequency Noise in MOS Transistors - I", Solid State Electronics, Vol. II (1968), pp. 797-812.

23. L. Boonstra and L. J. Sangster, "Analog functions fit neatly onto charge transport chips", Electronics, Feb. 28, 1972, pp. 64-71.

24. M.G. Kovac, W.S. Pike, F.V. Shallcross and P.K. Weimer, "Solid state imaging emerges from charge transport", Electronics, Feb. 28, 1972, pp. 72-77.

25. R. S. C. Cobbold, Theory and Applications of Field Effect Transistors, John Wiley and Son, New York: 1970.

26. R. L. Powell and W. A. Blanpied, "Thermal Conductivity of Metals and Alloys at Low Temperatures", National Bureau of Standards Circular No. 556 (September 1954), p. 36.

27. W. L. Wolfe, "Optical Materials", in Handbook of Military and Infrared Technology, W. L. Wolfe, Ed., Office of Naval Research, Department of the Navy, Washington, D. C., 1965, Ch. 8.

28. T. Limperis, "Detectors", in Handbook of Military and Infrared Technology, W. L. Wolfe, Ed., Office of Naval Research, Department of the Navy, Washington, D. C., 1965, Ch. 11.

APPENDIX A
SOURCES OF THE MATERIALS USED IN THE PRESENT PROJECT

Material	Source
1. Apiezon Black Wax	Apiezon Products, Ltd., England. Distributed in the United States by the James G. Biddle Co., Plymouth Meeting, Pennslyvania.
2. Catechol	Eastman Organic Chemicals, Eastman Kodak Company, Rochester, N. Y. 14650, Catalog No. 604, "Pyrocatechol".
3. Ethylenediamine	Eastman Organic Chemicals, Eastman Kodak Company, Rochester, N.Y. 14650, Catalog No. 1915, "Ethylenediamine".
4. GAF PR-115 Photoresist and its associated developer.	Commercial Development Dept., GAF Corporation, 140 W. 51st St., New York, N.Y. 10020.
5. G.E. Glyptal 1201 Red Enamel	General Electric Company, Schenectady, New York 12306.
6. G.E. Silicone Resin SR-319	General Electric Company, Schenectady, New York 12306.
7. Glycine	Nutritional Biochemicals Corp., 26201 Miles Road, Cleveland, Ohio 44128, "Ammonia Free Aminoacetic Acid".
8. Glycolic acid	Fisher Scientific Company, 52 Fadm Rd., Springfield, N.J. 07081, Catalog No. A-130, "Glycolic Acid - Purified".
9. J-100	Indust-Ri-Chem Laboratory, 726-32 South Sherman St., Richardson, Texas 75080, "Resist Strip J-100".
10. Kodak KTFR Photoresist and its associated developer and rinse	Eastman Kodak Company, Rochester, N.Y. 14650, "Kodak Thin Film Resist".

11. Microstop	Michigan Chrome and Chemical Co., 8615 Grinnel Ave., Detroit, Mich. 48213, "Microstop Stop-Off Lacquer".
12. RCA Resist	A proprietory photoresist made by RCA.
13. Shipley 1350 and its associated developer	Shipley Company, Inc., Newton, Mass. "Azoplate AZ-1350".
14. (110) Oriented silicon wafers polished on both sides	Electronic Materials Dept., Monsanto Company, St. Peters, Mo. 63376
15. Silicone oil	Dow Corning Corporation, Midland, Michigan, "Dow Corning 200 Fluid", a dimethylpolysiloxane with a viscosity of 100 cs. at 25 C.
16. Tetramethylguanidine	Eastman Organic Chemicals, Eastman Kodak Company, Rochester, N.Y. 14650, Catalog No. P8288, "1,1,3,3-Tetramethylguanidine".
17. Triglycine sulfate	Eastman Organic Chemicals, Eastman Kodak Company, Rochester, N.Y. 14650, Catalog No. 9921, "Glycine Sulfate".

All other materials mentioned in this report and not listed above (e.g., solvents and other standard laboratory chemicals) were the standard reagent grade (or better) chemicals that are available from a number of vendors (e.g., Fisher Scientific Company, J.T. Baker Chemical Co., or Mallinckrodt Chemical Works).

APPENDIX B
MEASURED SOLUBILITY OF TGS IN VARIOUS LIQUIDS

Solubility is given in grams per liter at room temperature.

Ethylene glycol	3.2
Freon TF	0.07
Formic acid (88%)	160.0
GAF PR-115 photoresist	>0.03
GAF PR-115 developer	320.0
Hydrazine (97%)	430.0
Isopropyl alcohol	0.4
KPR Photoresist developer	>0.03
KTFR Photoresist developer	0.03
KTFR Photoresist rinse	>0.03
Methyl alcohol	2.6
Shipley 1350	0.03
Trichloroethylene (boiling)	0.01
Water	330.0

See Appendix A for the source of the various liquids listed.

APPENDIX C

PERIODIC HEAT FLUX ACTING UPON A THIN, SEMI-INFINITE SLAB

The problem of a line source with a periodic flux input is considered by Carslaw and Jaeger.* The specific form taken is of a bar heated at one end and radiating from the sides. They show that if the radiation loss from the bar is included in the heat conduction equation in the form

$$\frac{\partial T}{\partial t} = D \frac{\partial^2 T}{\partial x^2} - aT$$

a transformation of the type

$$T = ue^{-at}$$

converts the equation to a normal heat diffusion equation. The boundary condition of interest is of alternating heat flux in and out for periods τ so that

$$\frac{\partial T}{\partial x} = g(t) \quad (x = 0)$$

where g(t) is a square wave. The solution of the above equations for a periodic flux impressed from time 0 to t is

$$T = (D/\pi)^{1/2} \int_0^t g(t-z) e^{-(az+x^2/4Dz)} dz/z^{1/2} \qquad \text{(C-1)}$$

The above integral has been computed as a function of the dimensionless distance parameter $x(\pi/2D\tau_f)^{1/2}$ when g(t) is a square wave of period $2\tau_f$ in the steady state case, that is, when t is large. Figure C-1 shows the resulting form of the temperature variation for two phases of the input flux, the temperature being scaled by

$$(D/\pi)^{1/2} \quad (F/K)$$

*H.S. Carslaw, J.C. Jaeger, Conduction of Heat in Solids, 2nd ed. Oxford: University Press, 1959, pp. 76, 134.

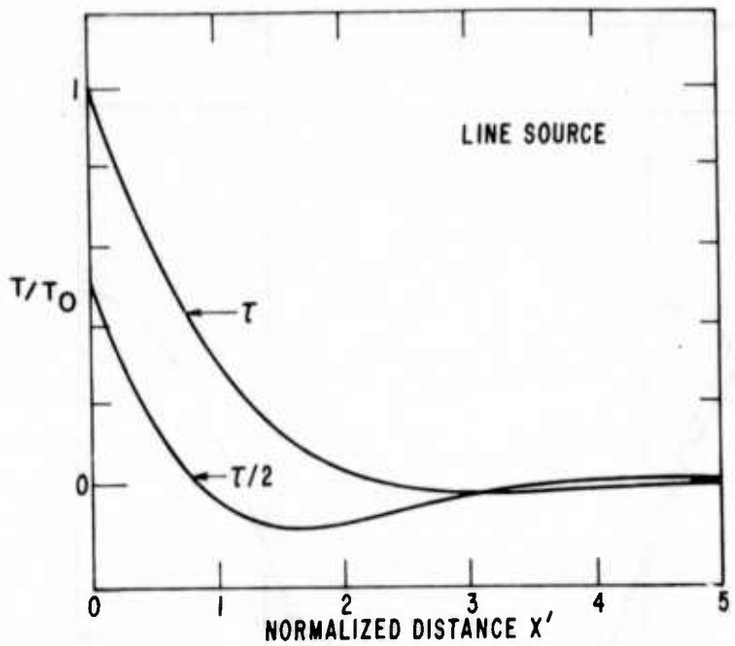


Fig. C-1. Temperature distribution in a thin sheet due to square-wave time-varying flux into a line source, as a function of the normalized distance $x' = x(\pi/2D\tau_f)^{1/2}$. Temperatures shown at end of exposure period and halfway through.

where F is the input flux variation amplitude and K the thermal conductivity. The radiation loss in this case is that due to black body radiation from the surface of the heat stored in the sheet of thickness d and volume specific heat C_v, so that

$$a = 8\sigma T^3/dC_v.$$

In fact, this heat loss, normally of the order of $0.3\ s^{-1}$, has very little effect on the form of the temperature distribution; its inclusion in the integral of Eq. (A-1) is convenient since it produces a reasonably rapid convergence of the integral which otherwise would have the slowly converging form $g(t-z)/z^{1/2}$.

The heat distribution from an arbitrary spatial pattern may now be found by integrating these line-source contributions. The results are shown in Figs. A-2 and A-3 for bar patterns of two different spacings. Temperature distributions at the end of frame exposure and half way through are shown as well as that which would result if there were no thermal diffusion. It can be seen that the spatial resolution limit occurs for a line-pair spacing of

$$\delta = 2.9\ (D\tau_f)^{1/2}.$$

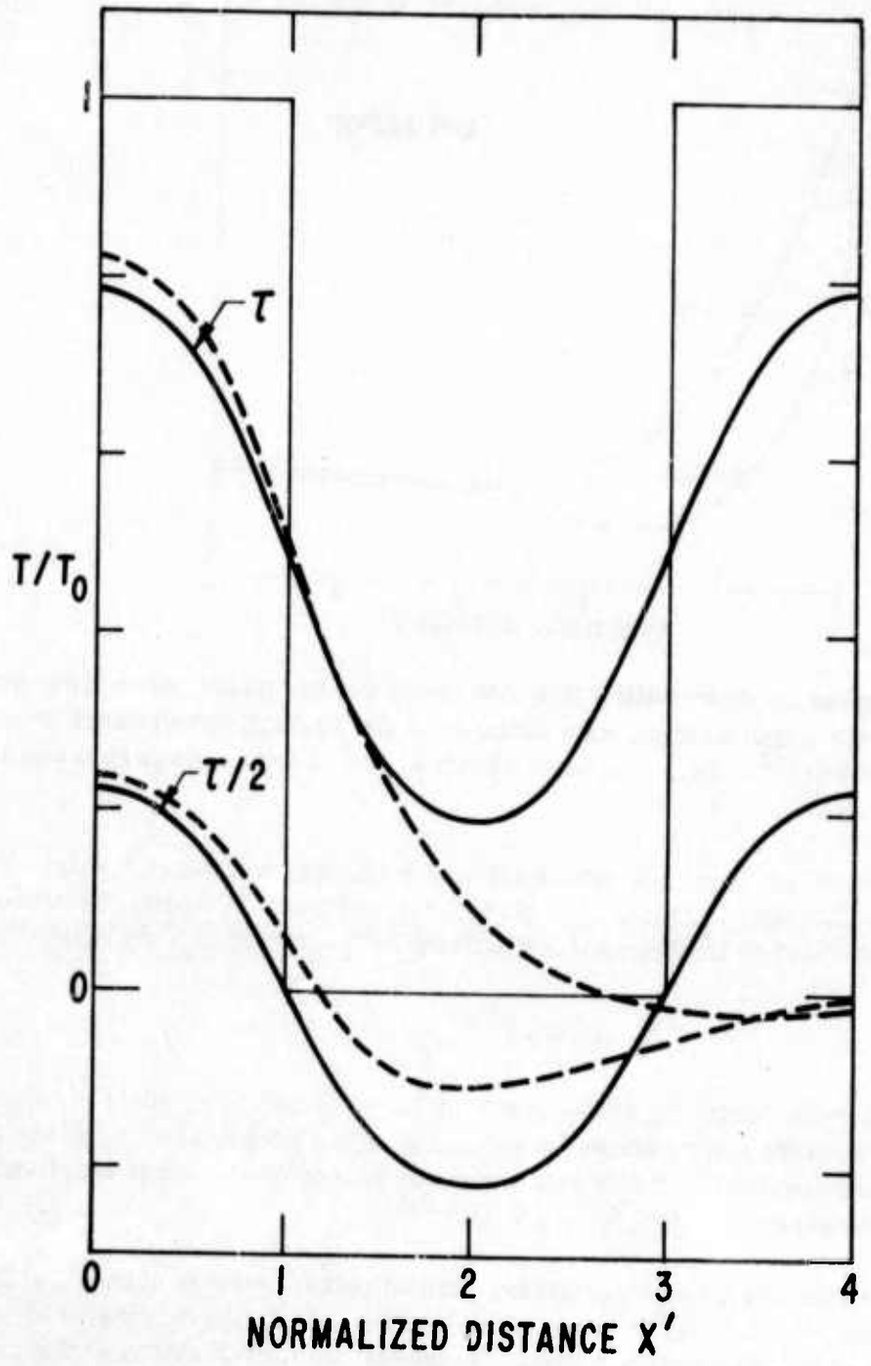


Fig. C-2. Temperature distribution from periodic bar pattern (solid) and single bar (dashed) (as in Fig. C-1). Bar width 2.0 normalized units. Square distribution is that in absence of thermal diffusion.

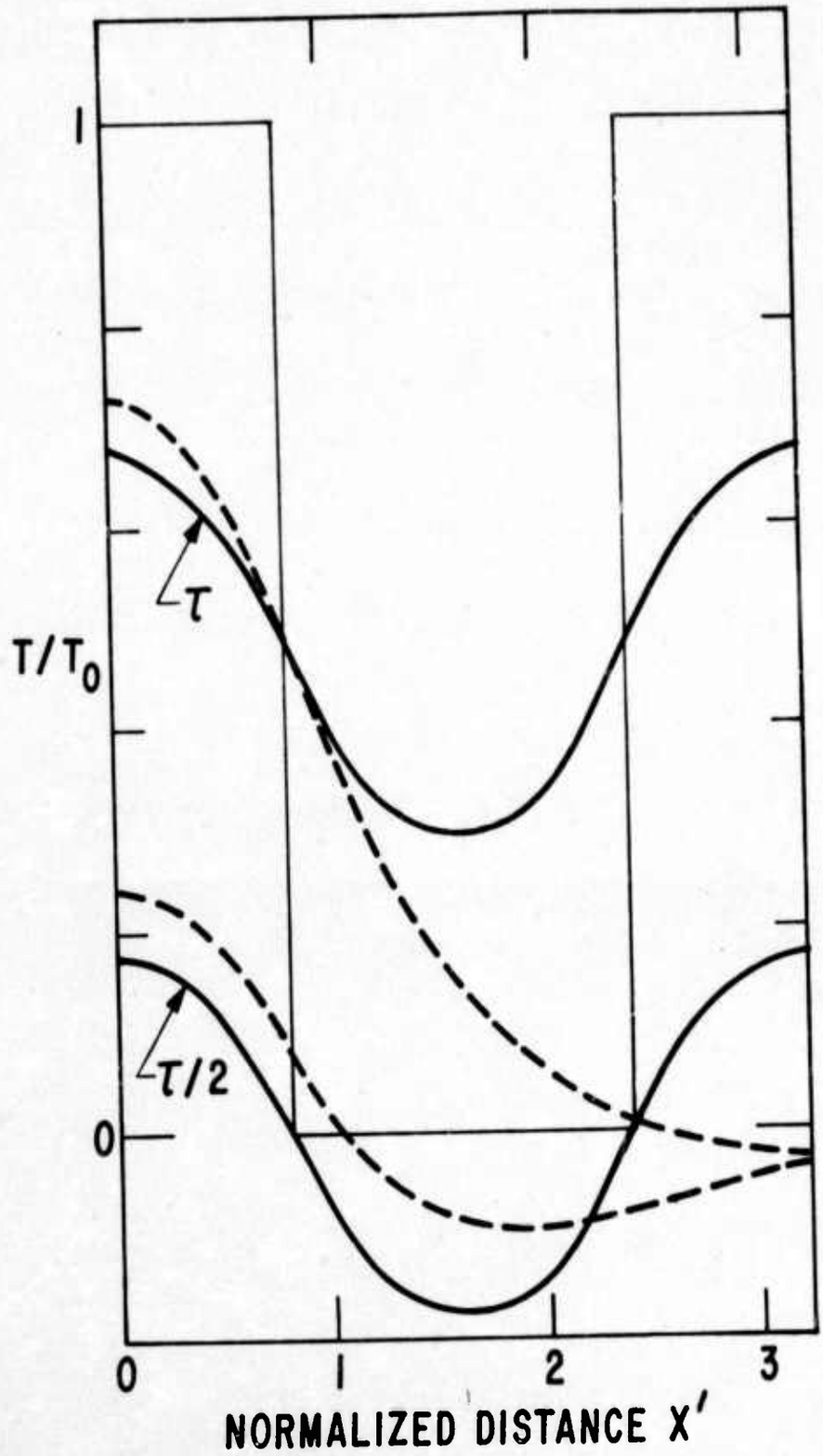


Fig. C-3. Temperature distributions for a bar width of 1.6 normalized units, as in Fig. C-2.

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13. ABSTRACT

The development of techniques leading to the fabrication of thin polycrystalline triglycine sulfate films and their resulting characteristics as infrared detectors are described. The processing technology required to fabricate pyroelectric/integrated circuit thermal imaging arrays consisting of thin film triglycine sulfate detectors on field effect integrated circuits is reviewed. The primary approach pursued under this program to the problem of providing the required high degree of thermal isolation between the detectors and the silicon substrate was to preferentially etch away the silicon underlying the detectors. In the resulting configuration, the thin thermally grown silicon dioxide membrane remaining after the etching process serves to support the detector. A second thermal isolation technique, in which a thin, permanently poled, single crystal section of TGS is positioned above its companion two-dimensional integrated circuit substrate, is also described. In this arrangement the resulting air gap provides the thermal isolation; contacts to the array detectors are made by means of vacuum deposited microfinger springs. The problem of providing thermal isolation proved to be the most difficult obstacle encountered during the program. No completely satisfactory approach evolved; as a result the objective of quantitatively assessing the performance of a small (16-by-16) element image sensor array was not met. The relative merits and shortcomings of X-Y and bucket brigade addressed pyroelectric sensor arrays are reviewed. The bucket brigade approach is shown to be a workable concept, with one 16-by-16 bucket brigade array having been fabricated and qualitatively assessed. An analysis of the performance capabilities of X-Y and bucket brigade addressed thin film pyroelectric arrays is performed.

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Infrared image sensor arrays						
Solid state scanning						
Pyroelectric detector array performance						
Laser evaporation						